GOI ESKOLA POLITEKNIKOA
FACULTY OF ENGINEERING

Ph.D. THESIS

PREDICTIVE CONTROL OF THE 2L-VSI AND 3L-NPC VSI BASED ON DIRECT POWER CONTROL FOR MV GRID-CONNECTED POWER APPLICATIONS

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Abstract

This dissertation proposes a new control approach, called Predictive Direct Power Control (P-DPC), where the well-known direct power control is combined with a predictive selection of a voltage-vectors sequence, obtaining both high transient dynamic and constant switching frequency. Different P-DPC versions are developed based on an optimal application of two, three, symmetrical 2+2 and symmetrical 3+3 voltage vectors' sequences. This control algorithm is compared to standard voltage oriented control (VOC) strategies under two of the most widely employed VSI-based configurations; the three-phase two-level VSI and the three-level NPC VSI. Several simulation and experimental results show that the P-DPC improves the transient response and keeps the steady-state harmonic spectrum at the same level as the VOC strategies. Due to its high transient capability and its constant-switching behavior, the P-DPC could become an interesting alternative to standard VOC techniques for grid-connected converters.

Keywords
DC/AC power conversion, Inverters, Predictive Control

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Chapter 1

1. Introduction

1.1. State of the Art

During the last ten years Medium and Low Voltage grids have been interconnected to a large number of new active systems such as wind turbines, hydraulic generators, biomass and geothermal generators, photovoltaic systems, fuel cells, storage devices, power quality improvement units (FACTS, D-FACTS, etc.) and others. Almost all of these new installations are interconnected to the grid by means of a Voltage Source Inverter (VSI) and a filter [1-3]. The three-phase two-level VSI based on PWM has usually been employed as a robust and highly efficient solution, becoming very popular mainly in Low Voltage (LV) levels. However, over the last few years, increasingly there has been an interest to develop high-power multi-level VSIs directly connected to Medium Voltage (MV) grids[3]. Generally these devices must provide a target active and/or reactive power level to the line, requiring appropriate Power Control systems.

The use of high-power electronics is being extended to different systems related to power generation, industrial equipments, traction applications etc. Among generation systems, for instance, wind energy stands out, which has been widely developed across Europe and in particular in Spain. This expansion is due to good economic conditions in renewable energies and research efforts carried out in this field. Therefore, wind turbines are now widely-used energy suppliers offering a cost effective option in the energy market [4;5]. Thus, variable speed technologies based on low/medium power VSI (<600kW) have been very common in wind farms [6;7]. In fact, the number of wind turbines which compose of a wind farm tends to decrease but at the same time increasing the rated power in each one of them. Consequently, there has been an increase of 750kW per unity installed to 3MW at the end of the nineties, or even to 5MW in the next few years [8;9]. These powers produce a remarkable increase of line currents under low voltage lines (which typically are connected), raising the installation costs and making the design aspects as size of filters, wires and other system's devices difficult. Therefore, the wind sector shows a big interest in the direct connection of these units to MV levels for future developments [10].

On the other hand, the liberalization of the electric market is stimulating new concepts as power quality which includes the continuous energy supply and wave quality importance [11;12]. The distribution and transport grids are usually based on air-lines and are very susceptible to weather hardness, uncontrollable actions and their inner performance effects. As well as that, the low energy-quality received by a customer can affect its vulnerable equipment (such as computers, automatic processes, etc.), leading to considerable economic damage. This problem forces to install new equipments in order to improve the power quality in the medium and low distribution grids, which are usually based on high-power VSI controlled by means of Digital Signal Processors (DSP). These devices, so-called *CUSTOM POWER* or *Distribution FACTS (D-FACTS)*, can have different performances as active filters, reactive energy compensators, protection against grid voltage dips or interruptions, etc[13-15].

Other sectors such as electric-based traction and electric drive industries are also supporting high-power electronic-based developments. Though these applications present different features compared to grid-connected systems, a large number of solutions for high power and medium voltage equipments have been developed [1;16-21].

1.1.1. High Power Electronics for MV Applications

Nowadays, improvements in the new semiconductors such as the increase of tolerable voltage around some kV, the capability of high currents and fast switching performances allow us to make an efficient design of VSI for MV applications. These improvements are mainly based on new developments in the semiconductor's features related to thyristors and transistors. Among the new semiconductors it is possible to find the improved GTO (*Hard Driven GTO o GCT*), the IEGT, the IGBT and the IGCT are commercially available. The last two devices are becoming the best options for future medium voltage and high-power applications[1;22;22-26]. The maximum nominal voltage and current ratings of these devices are shown in Fig. 2.2.

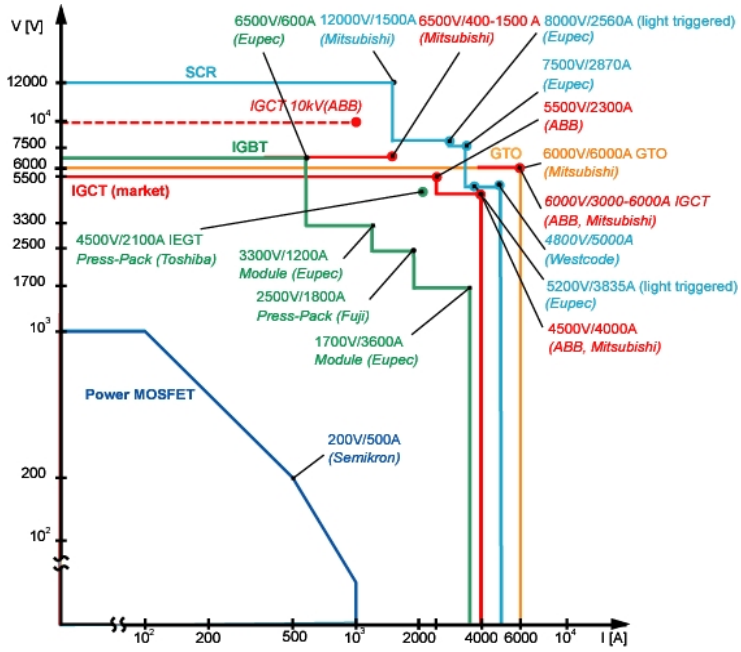


Fig. 1.1: Maximum nominal voltage and current ratings of available gate controlled power semiconductors [1]

The different features of IGBTs and IGCTs differentiate them and make each device attractive for a given family of applications. An interesting study has been carried out in [1], giving a classification of these devices depending on their operation ranges, see Fig.1.2. Here, the LV-IGBT ($V_{CE} \leq 1700V$) modules cover a large part of the low voltage drives market under line-voltages between 200V and 690V. The HV-IGBT ($V_{CE} \leq$ 2500V-6500V) are very competitive for the design aspects of VSI ranging from few power ratings (200kVA) to several MVA (5-7MVA) between 1kV and 7.7kV line-voltages. The IGCT clearly dominates the market between 2.3kV and 15kV under high-power ratings (3-100MVA). Finally, the IGBT *Presspack* is mainly employed in HVDC transmission systems where a redundant converter design is the main requirement and each converter's switch position consists of parallel connection of several stacks formed by the series connection of many IGBTs.

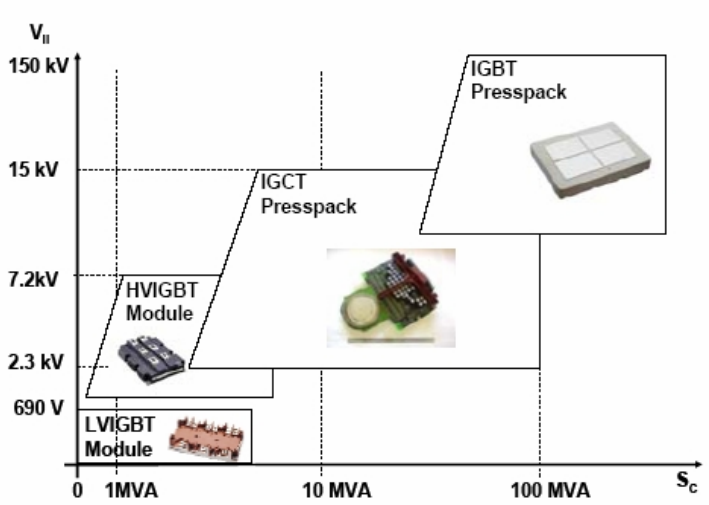


Fig.1.2: Operation ranges in IGBTs and IGCTs [1]

1.1.2. Medium Voltage Power Converters

The three-phase two-level VSI configuration is the most habitual topology employed in many applications because of its simplicity, reliability and robustness. Over a number of years they have frequently been employed in the wide market of electrical drives, becoming very popular in the industrial sector. Generally, almost all of the high-power VSI units used under medium voltage applications have been based on thyristors and GTOs [27;28].The main reason is the high voltage and current levels which allow these kinds of devices. However, the switching frequency is limited to a few hundred Hz, leading to employ bulky and expensive line filters. As a result there are more and more medium-high power systems, which have usually been developed based on conventional technologies (Thyristors, GTOs, etc.) that tend to be replaced in order to operate with higher switching frequencies and minimize the cost related to the filter size [1].

In addition to this, there are many applications which have been connected to medium voltage grid by means of a VSI, such as some variable speed systems (mainly wind and hydraulic generation) and FACTS devices (active filters, flicker compensators, Dynamic Voltage Restorers etc.). These devices operate at low voltage levels along with a coupling transformer which allows the connection to medium voltage levels [2;5;8;13;29]. In fact, they can operate at medium/ high switching frequencies (2-5kHz) operating under PWM-type modulations. This configuration presents some advantages from the viewpoint that it is possible to use low voltage devices in such a way that good steady-state and transient behavior is obtained. In spite of this, the coupling transformer decreases the efficiency of the installation and usually presents a bulky size. Hence, the trend is to use the new state of the art of semiconductors and the multilevel topologies to connect the VSI directly to MV levels [3]. To sum up, the main aim of these activities is to obtain higher efficiency levels decreasing the size of the grid-filter and/or avoiding the coupling transformer.

The new VSI developments for medium voltage applications are mainly based on IGCTs of 4.5kV, 5.5kV and 6.5kV or HV-IGBTs of 3.3kV, 4.5kV and 6.5kV. Thus, it is for example possible to design two-level-based VSIs suitable for 4.2kV and some few MVAs (2-7MVA) using stack topologies (based on series connection of 3.3kV HV-IGBT) and operating under medium switching frequencies (below 2 kHz) [27;28]. In spite of this, a coupling transformer is still required or a multi-level design must be adopted.

The multi-level structures appear in order to increase the power of VSI by means of adding voltage levels in such a way that the voltage in each semiconductor is reduced. Any VSI is considered as a multi-level converter if the voltage between whichever of the converter's output phase and any point of the DC-link has three or more levels. Generally, a larger number of voltage levels applied to a given filter make it decrease the harmonic range of the current, obtaining a high power quality in the converter's AC-side. The augmentation on voltage levels can be obtained increasing the number of switches, which leads to complex structures and, as a consequence, makes the control difficult. The features of these topologies are very attractive for many applications, involving the sector of VSI for medium voltage and high-power in particular. The main multi-level converter's topologies are: the Neutral Point Clamped (NPC), the cascaded H-Bridge and the Flying Capacitors (Multicell).

There are several interesting studies comparing these topologies on the basis of some design requirements as voltage levels, cost, power quality, switching and conduction losses and others [30-36]. However, commercially the three-level NPC-based technology is one of the most utilized. Manufacturers as ABB, Siemens, Alstom, and AsiRobicon typically offer these kinds of units for electrical drives in applications such as petrochemical, mining, steel, cement, paper production etc. For instance, ABB proposes the ACS 1000 and ACS 6000 based on IGCTs for medium voltage levels (2.3-3.3kV) and power ratings between 0.3kW and 27MW. On the other hand, Siemens offers SIMOVERT ML2 and SIMOVERT MV using IGCT-based technology for 3.3-6.6kV voltage levels under 4-7.5MW power ratings. In a similar way, AsiRobicon has developed the SILCOVERT TN and SILCOVERT GN products based on HV-IGBTs and IGCTs for voltage levels between 2.4-4.2kV under 1.2-20MW power ratings.

The Multicell technology is less popular because it has been patented by only one manufacturer (Alstom). The ALSPA VDM product based on IGBT and GTO technologies competes against other ABB, Siemens and AsiRobicon products under power ratings of 0.5-9MW and between 2.4kV and 6.6kV. Also, the cascaded H-bridge has been developed among others by AsiRobicon under the PERFECT HARMONY series with LV-IGBT technology. These VSI can be used between 2.3kV and 13.8kV under power ratings from 0.3MW to75MW.

1.1.3. Indirect and Direct Control Strategies

As is well-known, grid-connected VSI-based systems are able to control the power flow providing high efficiency and reliability levels. Generally, the control techniques which are commonly used could be classified as direct or indirect control strategies see Fig.1.3. The indirect control is characterized by a modulator (Pulse Wide Modulation PWM or other) that computes the turn-on/turn-off times of the converter's switches along a switching period through the evaluation of the voltage reference. This voltage reference is issued by the controller, which idealizes the converter as a dependent continuous voltage source. On the other hand, direct control techniques establish a direct relation between the behavior of the controlled variable and the state of the converter's switches.

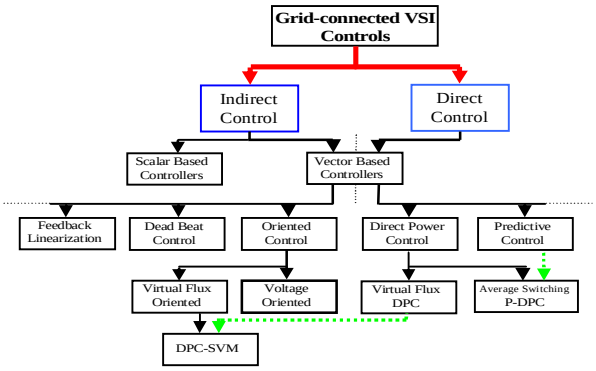


Fig.1.3: Classification of control techniques used in grid-connected VSIs

1.1.3.1. Indirect Power Control Techniques

Though there are many strategies to control the grid-side converters, summarized in Fig.1.3, the indirect-control type Voltage Oriented Control (VOC) is mainly utilized [37-42]. It is based on the knowledge of the position of the line-voltage vector and the relative spatial orientation of the current vector. It employs the well-known Park's transformation to a rotating *dq0* reference frame aligned with the line-voltage or the Clark's transformation to a static *αβ0* reference frame, see Fig.1.4.

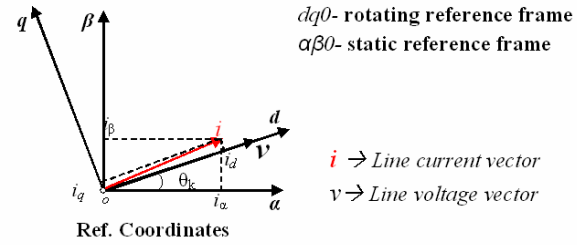


Fig.1.4: Graphical representation of VOC-based reference coordinates

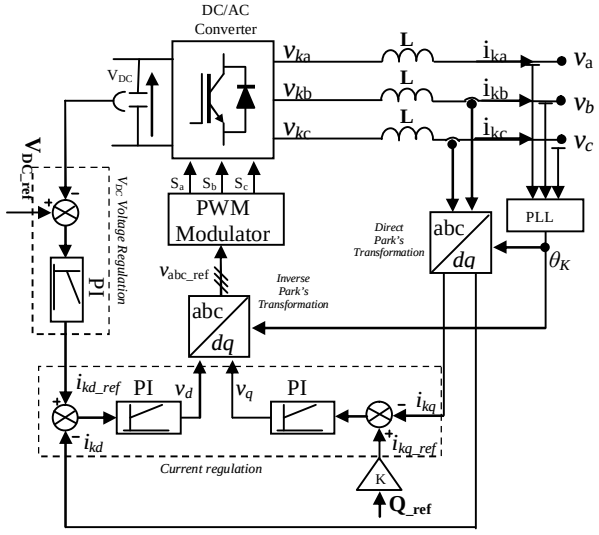


Fig.1.5: Block diagram of VOC in rotating *dq* reference frame

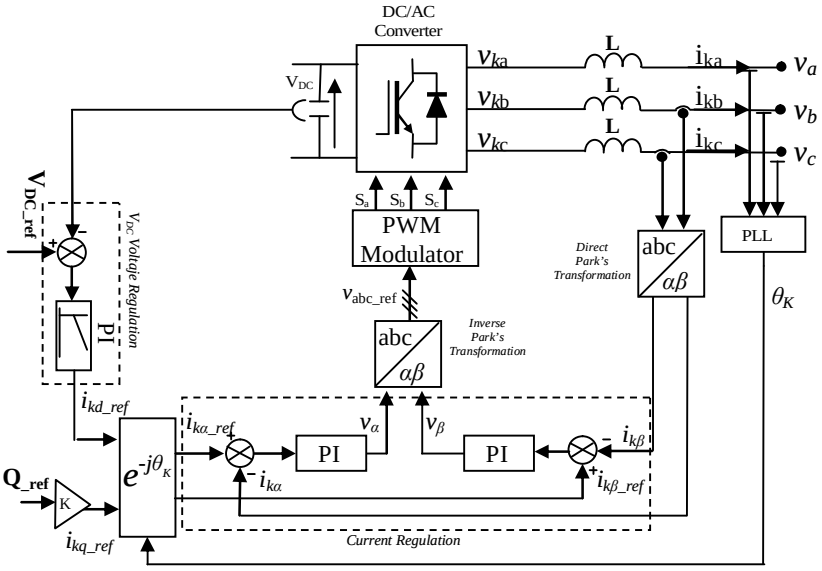


Fig.1.6: Block diagram of VOC in static *αβ* reference frame

Recent developments have popularized the Virtual Flux (VF) concept, which assumes that both the grid and converter's line filter behave as an AC motor, see Fig.1.7. Thus the resistance and the inductance of the filter are equivalent to the phase resistance and the leakage inductance of the motor, whereas the phase voltage of the converter is related to a fictitious virtual flux [43;44]. One of the main advantages of this new approach is that it is less sensitive to line-voltage variations than other approaches. The Virtual Flux Oriented Control (VFOC) is an adaptation of the VOC to a VF reference frame [43-45], see Fig.1.8.

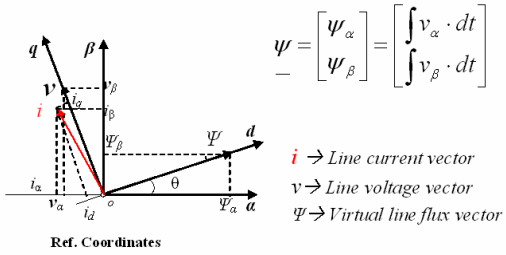


Fig.1.7: Graphical representation of VF-based reference coordinates

Indirect control strategies generally lead to good transient behavior and acceptable steady-state operation. They operate at a constant switching frequency, which makes the use of advanced modulation techniques possible. Therefore, it becomes easier to optimize conversion power losses or to simplify the line-side filter design.

Otherwise, these control techniques have some disadvantages. The main problem is common in any indirect control strategy under a PWM-type modulation: if the ratio between switching and grid-fundamental frequencies is not large enough, the VSI can not be considered as an ideal controlled continuous voltage source. In these conditions, it becomes impossible to use the notion of the converter's average voltage vector in control requirements.

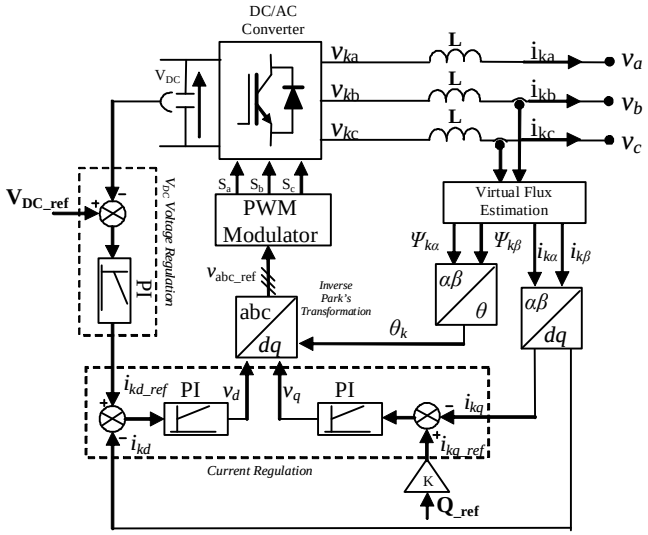


Fig.1.8: Block diagram of VFOC

1.1.3.2. Direct Power Control Techniques

Direct Power Control (DPC) is one of the most popular direct control strategies of grid-connected converters [43;44;46-49]. This technique is derived from the first and original Direct Torque Control (DTC) of AC machines. In each sampling time it evaluates which one of the instantaneous voltage vectors (available at the output of the converter) is best suited in order to push the state of the system towards the reference value. As this evaluation is continuously carried out, direct control technique does not require any modulator and it is able to get the maximum dynamic capability available in the system. Moreover, it does not require any internal control loop or any coordinate transformation, avoiding coupling effects between transformed variables. In the DPC case, instantaneous active and reactive power control loops are based on hysteresis regulators that select the appropriate voltage vector from a look-up table, see Fig.1.9.

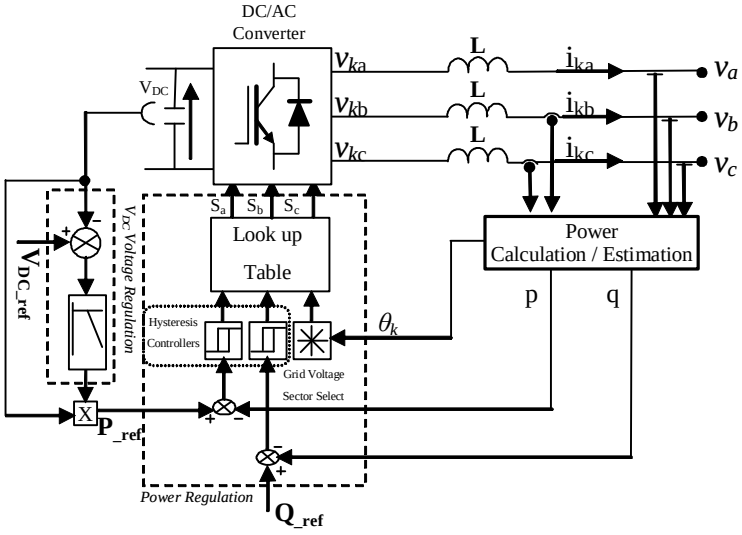


Fig.1.9: Block diagram of DPC

The DPC technique has also been implanted under the VF concept, leading to the Virtual Flux Direct Power Control (VF-DPC)[43;44], see Fig.1.10.

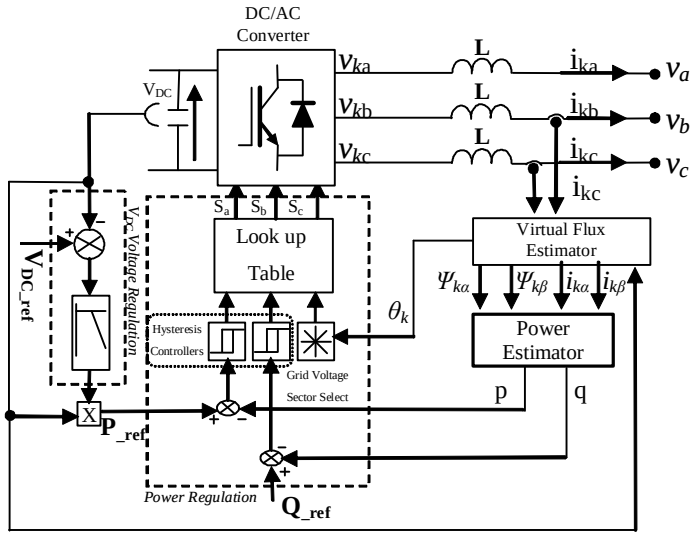


Fig.1.10: Block diagram of VF-DPC

The main disadvantage of the DPC strategy is the resulting variable switching frequency, which is usually not bounded and depends mainly on the sampling time, look-up table structure, load parameters and the state of the system. As a result, these kinds of controls generate a dispersed harmonic spectrum, making it difficult to design the line-filter in order to avoid possible grid resonances [50]. The mixed DPC-SVM approach is an adaptation of VFOC and VF-DPC techniques which provide the required converter's average voltage, also applied to the Space Vector Modulation (SVM) [51-56]. This strategy could be defined as a direct control method based on the fact that the converter's average voltage vector is *directly* computed using active and reactive power tracking requirements, see Fig.1.11. Nevertheless, in the frame of this thesis and taking into consideration that it uses a modulator, it should be classified as an indirect control strategy.

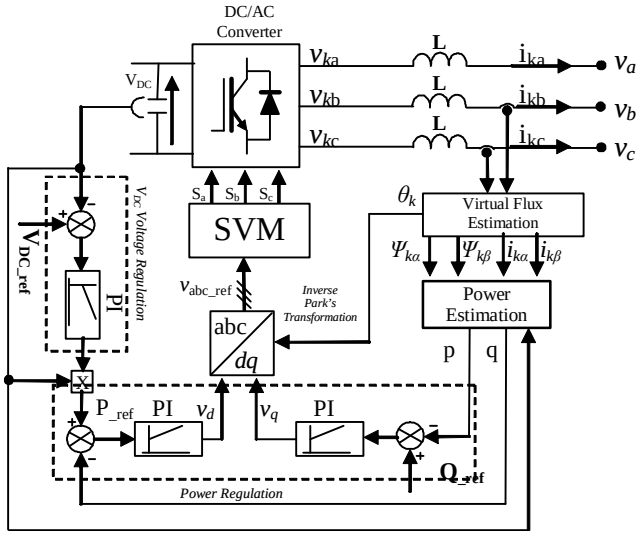


Fig.1.11: Block diagram of DPC-SVM

Predictive approaches have also been employed in order to overcome the variable switching frequency problem of the DPC strategy. These solutions have been mainly employed in the control of AC machines [57-61]. Instead of selecting an instantaneous optimal voltage vector (DTC-case), predictive type approaches select an optimal set of concatenated voltage vectors, the so-called "voltage-vectors' sequence". The control problem is solved computing the application times of the vectors of the sequence in such a way that the controlled variables converge towards the reference values along a fixed predefined switching period. This way constant switching frequency operation is obtained. Several authors have developed this concept in multilevel converter topologies linked to different kind of machines but there are few predictive control applications on line-connected VSI systems. Some authors propose predictive current control algorithms related to power control requirements but it results in variable switching frequency [62;63].

Some interesting work has been carried out related to line-current control where a sliding-control type approach is combined with predictive computing of voltage application times [64]. This way both high transient dynamics and constant switching frequency are obtained.

1.2. Scientific Contribution

The aim of this dissertation is to research and develop a new control approach for grid-connected VSI where DPC is combined with predictive vector sequence selection, obtaining both high transient dynamic and constant switching frequency. Therefore the following thesis can be formulated:

"A predictive control strategy for DC/AC converters based on Direct Power Control allows high transient dynamic under low switching frequency constraints for medium voltage grid-connected VSI, becoming an interesting alternative to VOC techniques."

In order to prove this thesis, the author has used analytical and simulation-based approaches, as well as experimental tests of a grid-connected two-level and three-level NPC VSI. In the author's opinion the original scientific contributions of this dissertation are:

- Definition of the theory of a new predictive algorithm based on Direct Power Control, the Predictive-Direct Power Control (P-DPC)
- Development of different versions of P-DPC: P-DPC based on two, three, symmetrical 2+2 and symmetrical 3+3 voltage vectors' sequences
- Simulation and experimental application to a two-level VSI
- Simulation and experimental application to a three-level NPC VSI
- Analysis of the overall operation performance against typical disturbances on the grid
- Analysis of the overall robustness against variations on the parameters of the grid-filter's

Other results that may not be original contributions, but are believed to be important technological developments or to have a significant practical value, are:

- Modelling of the dynamics of the instantaneous active and reactive powers of three-phase N-level VSI under rotating dq and static $\alpha\beta$ reference frames.

- Development of L-type filter design considerations based on low and high frequency requirements.

- Definition of the design procedure of controllers for power-control tasks using VOC and DPC strategies.

1.3. Thesis Outline

This thesis is divided into seven chapters which are summarized as follows:

Chapter 1. Introduction

This chapter describes the frame of this dissertation and formulates the problem which is discussed in this manuscript.

Chapter 2. Analysis and Design Considerations of 2L-VSI and 3L-NPC VSI for MV Grid-connected Power Applications

Chapter 2 describes the fundamental operation performances of the 2L-VSI and 3L-NPC VSI. Mathematical models and some design considerations are presented, extending these ideas in order to select the passive electric components for 2.3kV-2MVA operation conditions.

Chapter 3. Power Control Strategies for Grid-connected VSI-based Systems

Chapter 3 is focuses on two of the most interesting power control strategies for grid-connected VSI-based systems, the VOC and the DPC. In fact, some design considerations are defined for both control methods under 2L-VSI and 3L-NPC VSI configurations, showing the main features and requirements under the MV grid-connection operation condition.

Chapter 4. Predictive Direct Power Control

This Chapter defines the theory of a new predictive control approach based on the DPC, called Predictive Direct Power Control. Furthermore, different P-DPC versions are proposed, applying these concepts under the 2L-VSI and 3L-NPC VSI configurations. Some simulations of these strategies under 2.3kV-2MWA grid-connected operation conditions have been carried out.

Chapter 5. Control Operation Performance

This Chapter discusses the control operation performance of the most interesting control strategies for MV grid-connected applications. The behavior of these control strategies against parameter's uncertainty on line-disturbances is compared.

Chapter 6. Simulation and Experimental Results

Chapter 6 shows the simulation and experimental results which have been carried out in order to verify the proposed algorithms.

Chapter 7. Conclusions

Finally, this Chapter presents a brief summary containing the conclusion and proposing the future work related to this dissertation.

Appendix

This work is supplemented by the following appendices:

A.1. Coordinate transformations

A.2. Harmonic Limitation

Chapter 2

2. Analysis and Design Considerations of 2L-VSI and 3L-NPC VSI for MV Grid-Connected Power Applications

2.1. Introduction

The development of new kinds of high-power, medium voltage (MV) and fast switching semiconductors (as Integrated Gate Commutated Thyristors (IGCTs), High Voltage IGBTs (HV-IGBTs) etc.) combined with the utilization of Digital Signal Processors (DSPs) has stimulated direct MV connection of power converters in a large number of applications (wind turbines, hydraulic generators, biomass and geothermal generators, fuel cells, storage devices, FACTS, and others)[1;16;17;21]. Today, the two-level VSI (2L-VSI) and the three-level Neutral Point Clamped VSI (3L –NPC VSI) are two of the most widely used high power topologies [20].

In this chapter some principles of operation of grid-connected converters are discussed. Also, mathematical models and some design considerations of 2L-VSI and 3L NPC-VSI are shown, leading a generalized development of N-level NPC VSI. In addition, usually employed vector-based modulation techniques are described in order to take into consideration their influence in a grid-connected VSI configuration. Finally, these ideas are extended to design the passive electric components of 2L-VSI and 3L-NPC VSI topologies under 2.3kV-2MVA operation conditions.

2.2. Grid-connected Power Converters

Let us consider a generic per-phase line-connected VSI configuration as in Fig. 2.1. Where $\boldsymbol{v}$ shows a single-phase of symmetric three-phase voltages and represents the point of connection to the grid. The VSI is connected by means of a grid filter in order to reduce the current $\boldsymbol{i}$ harmonics and to fulfill the grid-connection standards. This device must provide a target active and/or reactive power level to the line, so it is able to control the phase and amplitude of the converter's AC-side both voltage $\boldsymbol{v_k}$ and current $\boldsymbol{i_k}$.

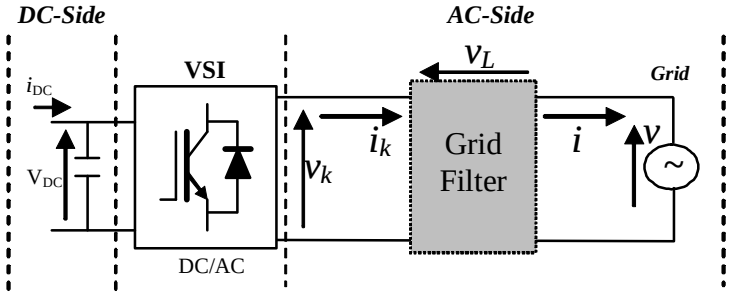


Fig. 2.1: Single-phase model of a line-connected VSI

Fig. 2.2 shows several examples of phasor diagrams (unity-power-factor and non unity-power-factor) of a VSI both when the power flows from the DC-side to AC-side (Inverter mode) and power flows from the AC-side to DC-side (Rectifier mode).

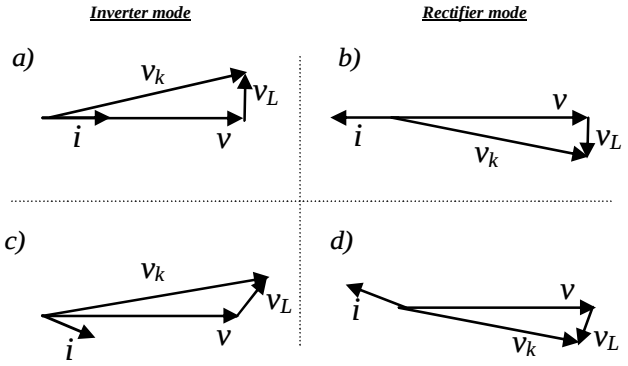


Fig. 2.2: Phasor diagrams: a,b) unity-power-factor operation. c,d) non unity-power-factor operation

There are many configurations for grid-connection based on different topologies of VSI which have been shown in Chapter 1. However, in the scope of this thesis 2L-VSI and 3L-NPC VSI topologies with an L-type grid filter will be considered.

2.2.1. 2L-VSI Configuration

The basic scheme of a grid-connected 2L-VSI with an L-type filter is shown in Fig. 2.3. The structure of the converter consists of six switching cells (based on IGBTs, IGCTs, GTOs, or others) in such a way that eight possible configurations of the switches are available, leading to seven possible voltage states at the output of the converter. Fig. 2.4 shows the available configurations of one switching leg of the converter. The output is connected to the negative (-) or positive (+) point of the DC-link when the state of the switch $\mathbf{S}_a$ is equal to '0' or '1', establishing a current way between the DC-side and AC-side.

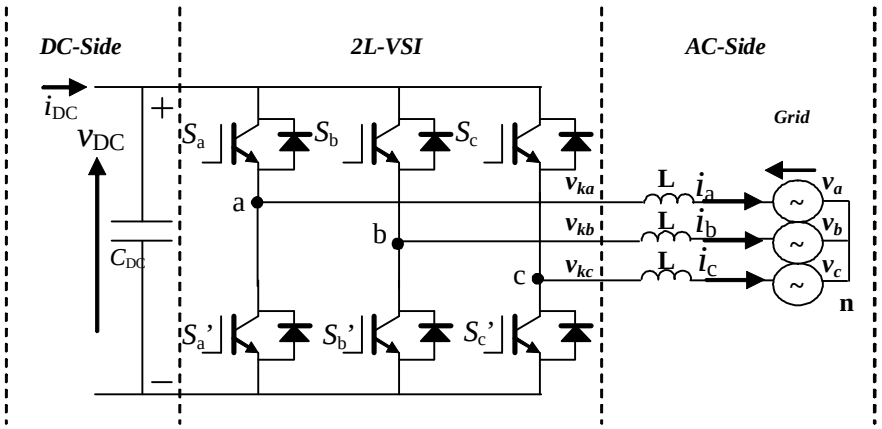


Fig. 2.3: Grid-connection of a three-phase 2L-VSI with a L-type filter

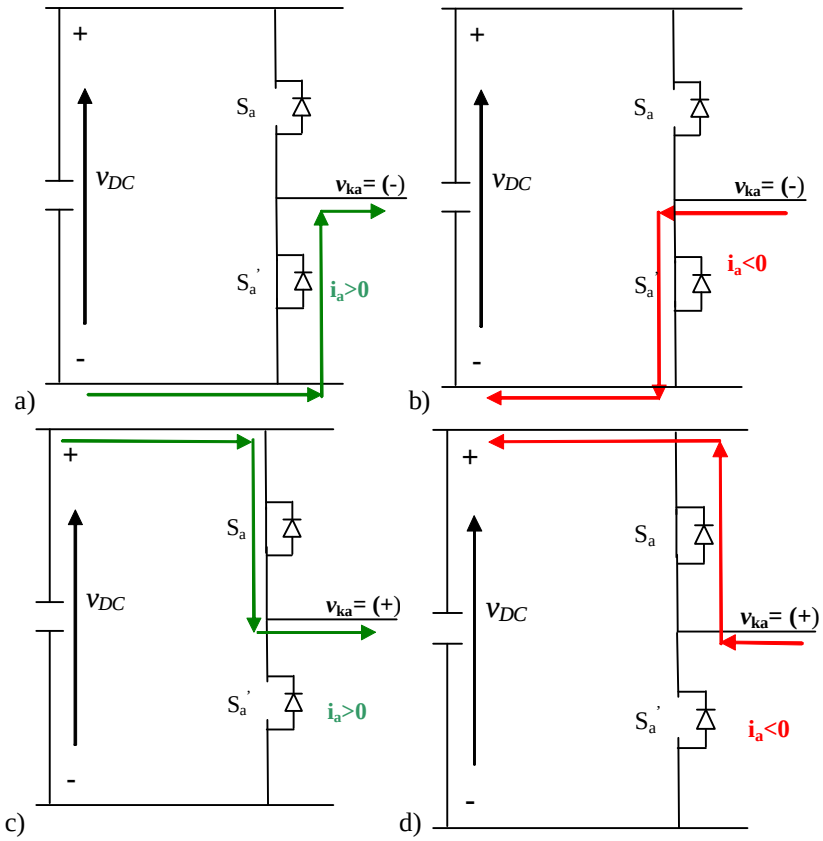


Fig. 2.4: Available switching states in the a-phase converter's leg – 2L-VSI: a) Sa=0 ia>0, b) Sa=0 ia<0, c) Sa=1 ia>0, d) Sa=1 ia<0

Equation (2.1) computes the available voltage vectors in the complex space. Six of them are classified as active vectors (the combination of the converter's switches leads to a non-zero voltage in the AC-side) whereas the other two vectors are null vectors (all phases are connected to the same point). The graphical representation is shown in Fig. 2.5.

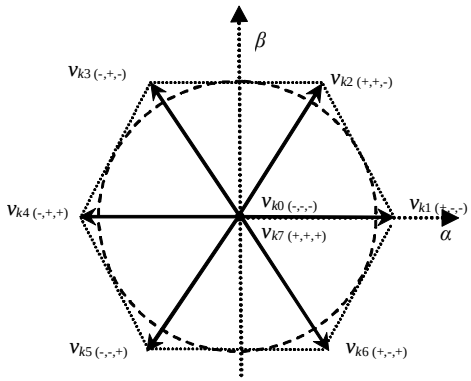


Fig. 2.5: Space vector representation of different voltage vectors available at the converter's AC-side in a 2L-VSI.

$$\begin{cases} v_{kn} = \frac{2}{3} v_{DC} e^{j(n-1)\frac{p}{3}} & n = 1,..,6 \\ v_{k0} = v_{k7} = 0 \end{cases} \tag{2.1}$$

Therefore, and assuming that the grid of Fig. 2.3 is a balanced three-phase power system, the following converter's per-phase equations related to the neutral point (**n**) of grid can be derived.

$$\begin{aligned} v_{ka} &= \frac{2S_a - (S_b + S_c)}{3} v_{DC} \\ v_{kb} &= \frac{2S_b - (S_a + S_c)}{3} v_{DC} \\ v_{kc} &= \frac{2S_c - (S_a + S_b)}{3} v_{DC} \end{aligned} \tag{2.2}$$

Equation (2.3) shows the per-phase dynamic behavior of the proposed power system, with $\boldsymbol{v_k}$ the converter's voltage, $\boldsymbol{v}$ the line-voltage and $\boldsymbol{i}$ the line-current vectors.

$$v_k = Ri + L\frac{di}{dt} + v \tag{2.3}$$

Also, the behavior of the DC-link voltage can be expressed based on the converter's switching pattern and AC-side currents. Then, it is possible to present the model of the system in the three-phase coordinates ***abc*** as follows:

$$\begin{cases} \frac{di_a}{dt} = -\frac{R}{L} i_a - \frac{1}{L} v_a + \frac{v_{DC}}{L} \left(\frac{2S_a - (S_b + S_c)}{3} \right) \\ \frac{di_b}{dt} = -\frac{R}{L} i_b - \frac{1}{L} v_b + \frac{v_{DC}}{L} \left(\frac{2S_b - (S_a + S_c)}{3} \right) \\ \frac{di_c}{dt} = -\frac{R}{L} i_c - \frac{1}{L} v_c + \frac{v_{DC}}{L} \left(\frac{2S_c - (S_b + S_a)}{3} \right) \\ C_{DC} \frac{dv_{DC}}{dt} = -(S_a i_a + S_b i_b + S_c i_c) + i_{DC} \end{cases} \tag{2.4}$$

In many applications it is useful to present the system model in static $\boldsymbol{\alpha\beta}$ or rotating $\boldsymbol{dq}$ reference frame, using the well-known Park's or Clark's transformations (Appendix). Equations (2.5) and (2.6) show the system behavior under the $\boldsymbol{\alpha\beta}$ and $\boldsymbol{dq}$ coordinates.

$$\begin{cases} \frac{di_a}{dt} = -\frac{R}{L} i_a - \frac{1}{L} v_a + \frac{v_{DC}}{L} f_a \\ \frac{di_b}{dt} = -\frac{R}{L} i_b - \frac{1}{L} v_b + \frac{v_{DC}}{L} f_b \\ C_{DC} \frac{dv_{DC}}{dt} = -\frac{3}{2} (f_a i_a + f_b i_b) + i_{DC} \end{cases} \tag{2.5}$$

$$\begin{cases} \dfrac{di_d}{dt} = -\dfrac{R}{L} i_d - w i_q - \dfrac{1}{L} v_q + \dfrac{v_{DC}}{L} f_d \\ \dfrac{di_q}{dt} = -\dfrac{R}{L} i_q + w i_d - \dfrac{1}{L} v_q + \dfrac{v_{DC}}{L} f_q \\ C_{DC} \dfrac{dv_{DC}}{dt} = -\left(f_d i_d + f_q i_q \right) + i_{DC} \end{cases} \tag{2.6}$$

Where the appropriate switching states are expressed as:

$$f_a = \frac{2S_a - (S_b + S_c)}{3}$$

$$f_b = \frac{1}{\sqrt{3}} (S_b - S_C)$$

With

$$f_d = f_a \cos(wt) + f_b \sin(wt)$$

$$f_q = f_b \cos(wt) - f_a \sin(wt)$$

2.2.2. 3L-NPC VSI Configuration

Fig.2.6 shows the scheme of a grid-connected 3L-NPC VSI with an L-type filter. The converter consists of twelve switching cells and six clamp diodes, leading twenty seven non-destructive different combinations of the states of the switches. Any given output phases of the converter can be connected to negative ($\mathbf{S}_{a1}$=0, $\mathbf{S}_{a2}$=0), neutral ($\mathbf{S}_{a1}$=0, $\mathbf{S}_{a2}$=1) or positive ($\mathbf{S}_{a1}$=1, $\mathbf{S}_{a2}$=1) points of the DC-link, which results in different current paths between the DC-side and AC-side. The allowed switching states are showed in Fig.2.7.

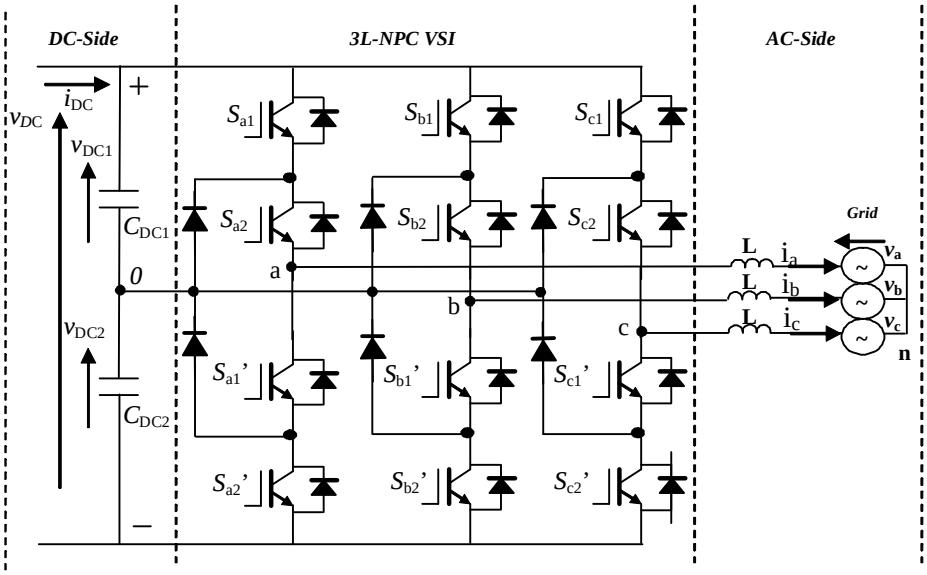


Fig.2.6: Grid-connection of a three-phase 3L-NPC VSI with a L-type filter

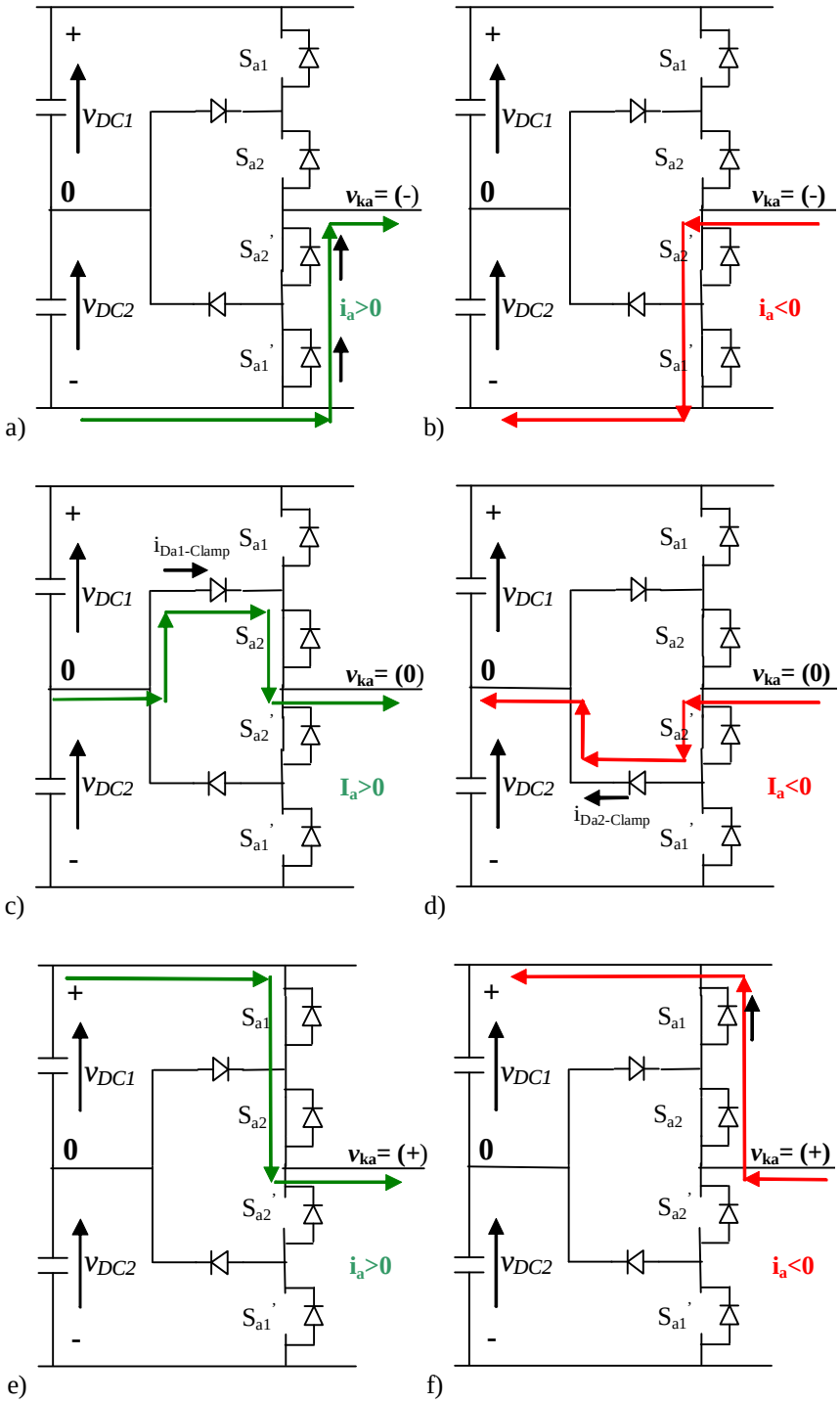


Fig.2.7: Available switching states in the *a*-phase converter's leg – 3L-NPC VSI: a) [S_{a1}=0, S_{a2}=0] i_a>0, b) [S_{a1}=0, S_{a2}=0] i_a<0, c) [S_{a1}=0, S_{a2}=1] i_a>0, d) [S_{a1}=0, S_{a2}=1] i_a<0, e) [S_{a1}=1, S_{a2}=1] i_a>0, f) [S_{a1}=1, S_{a2}=1] i_a<0

The twenty-seven switching states of the 3L-NPC VSI generate nineteen different voltage vectors at the converter's AC-side (eighteen active vectors and one null vector). The availability of redundancies in different states provides extra degrees of freedom. Equation (2.7) computes the vector representation in the complex space where the sub-index *l,m,s* are related to large, medium and small vectors .The graphical representation is shown in Fig.2.8.

$$\begin{cases} v_{kn\_l} = \frac{2}{3} v_{DC} e^{j(n-1)\frac{p}{3}} \\ v_{kn\_m} = \frac{1}{\sqrt{3}} v_{DC} e^{jn\frac{p}{6}} \\ v_{kn\_s} = \frac{1}{3} v_{DC} e^{j(n-1)\frac{p}{3}} \\ v_{k0} = v_{k1} = v_{k2} = 0 \end{cases} \quad n = 1,..,6 \tag{2.7}$$

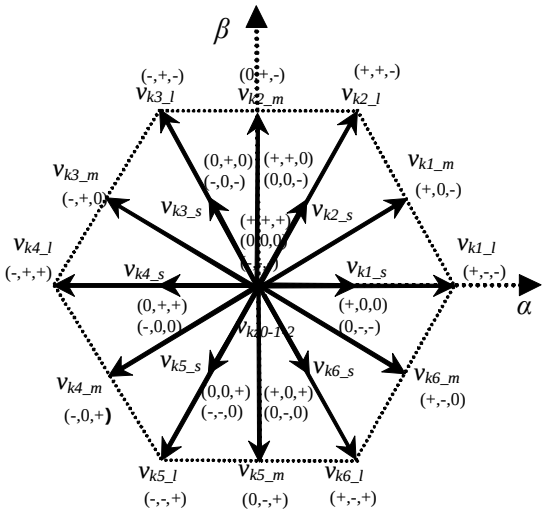


Fig.2.8: Space vector representation of different voltage vectors available at the converter's AC-side in a 3L-NPC VSI.

Assuming that the system shown in Fig.2.6 is a balanced three-phase power system, the following converter's per-phase equations related to the neutral point (**n**) of the grid can be derived.

$$\begin{aligned} v_{ka} &= \frac{2S_{a1} - (S_{b1} + S_{c1})}{3} v_{DC1} + \frac{2S_{a2} - (S_{b2} + S_{c2})}{3} v_{DC2} \\ v_{kb} &= \frac{2S_{b1} - (S_{a1} + S_{c1})}{3} v_{DC1} + \frac{2S_{b2} - (S_{a2} + S_{c2})}{3} v_{DC2} \\ v_{kc} &= \frac{2S_{c1} - (S_{a1} + S_{b1})}{3} v_{DC1} + \frac{2S_{c2} - (S_{a2} + S_{b2})}{3} v_{DC2} \end{aligned} \tag{2.8}$$

The line current behavior is defined in the same way as (2.3), whereas the DC-link voltage behavior must be related to each DC-link capacitor. Thus, the system mathematical model in the three-phase coordinates ***abc*** is defined as follows:

$$\begin{cases} \dfrac{di_a}{dt} = -\dfrac{R}{L}i_a - \dfrac{1}{L}v_a + \dfrac{v_{DC1}}{L}\left(\dfrac{2S_{a1}-(S_{b1}+S_{c1})}{3}\right) + \dfrac{v_{DC2}}{L}\left(\dfrac{2S_{a2}-(S_{b2}+S_{c2})}{3}\right) \\ \dfrac{di_b}{dt} = -\dfrac{R}{L}i_b - \dfrac{1}{L}v_b + \dfrac{v_{DC1}}{L}\left(\dfrac{2S_{b1}-(S_{a1}+S_{c1})}{3}\right) + \dfrac{v_{DC2}}{L}\left(\dfrac{2S_{b2}-(S_{a2}+S_{c2})}{3}\right) \\ \dfrac{di_c}{dt} = -\dfrac{R}{L}i_c - \dfrac{1}{L}v_c + \dfrac{v_{DC1}}{L}\left(\dfrac{2S_{c1}-(S_{a1}+S_{b1})}{3}\right) + \dfrac{v_{DC2}}{L}\left(\dfrac{2S_{c2}-(S_{a2}+S_{b2})}{3}\right) \\ C_{DC1}\dfrac{dv_{DC1}}{dt} = -(S_{a1}i_a + S_{b1}i_b + S_{c1}i_c) + i_{DC} \\ C_{DC2}\dfrac{dv_{DC2}}{dt} = -(S_{a2}i_a + S_{b2}i_b + S_{c2}\cdot i_c) + i_{DC} \end{cases} \tag{2.9}$$

The system representation in static ***αβ*** coordinates can be carried out as:

$$\begin{cases} \dfrac{di_a}{dt} = -\dfrac{R}{L}i_a - \dfrac{1}{L}v_a + \dfrac{v_{DC1}}{L}f_{1a} + \dfrac{v_{DC2}}{L}f_{2a} \\ \dfrac{di_b}{dt} = -\dfrac{R}{L}i_b - \dfrac{1}{L}v_b + \dfrac{v_{DC1}}{L}f_{1b} + \dfrac{v_{DC2}}{L}f_{2b} \\ C_{DC1}\dfrac{dv_{DC1}}{dt} = -\dfrac{3}{2}(f_{1a}i_a + f_{1b}i_b) + i_{DC} \\ C_{DC2}\dfrac{dv_{DC2}}{dt} = -\dfrac{3}{2}(f_{2a}i_a + f_{2b}i_b) + i_{DC} \end{cases} \tag{2.10}$$

Where the switching functions are:

$$f_{1a} = \frac{2S_{a1}-(S_{b1}+S_{c1})}{3}$$

$$f_{1b} = \frac{1}{\sqrt{3}}(S_{b1}-S_{c1})$$

$$f_{2a} = \frac{2S_{a2}-(S_{b2}+S_{c2})}{3}$$

$$f_{2b} = \frac{1}{\sqrt{3}}(S_{b2}-S_{c2})$$

On the other hand, the system can be represented in the following static ***dq*** reference frame.

$$\begin{cases} \dfrac{di_d}{dt} = -\dfrac{R}{L}i_d - wi_q - \dfrac{1}{L}v_q + \dfrac{v_{DC1}}{L}f_{1d} + \dfrac{v_{DC2}}{L}f_{2d} \\ \dfrac{di_q}{dt} = -\dfrac{R}{L}i_q + wi_d - \dfrac{1}{L}v_q + \dfrac{v_{DC1}}{L}f_{1q} + \dfrac{v_{DC2}}{L}f_{2q} \\ C_{DC1}\dfrac{dv_{DC1}}{dt} = -(f_{1d}i_d + f_{1q}i_q) + i_{DC} \\ C_{DC2}\dfrac{dv_{DC2}}{dt} = -(f_{2d}i_d + f_{2q}i_q) + i_{DC} \end{cases} \tag{2.11}$$

With

$$f_{1d} = f_{1a}\cos(wt) + f_{1b}\sin(wt)$$
$$f_{1q} = f_{1b}\cos(wt) - f_{1a}\sin(wt)$$
$$f_{2d} = f_{2a}\cos(wt) + f_{2b}\sin(wt)$$
$$f_{2q} = f_{2b}\cos(wt) - f_{2a}\sin(wt)$$

2.2.3. N-Level-NPC VSI Configuration

It is possible to develop a generalized model of N-level-NPC VSI. Fig.2.9 shows an example of a converter's leg where N^3 possible switching states can be generated. Considering a balanced grid, converter's per-phase equations related to the neutral point are derived in (2.12).

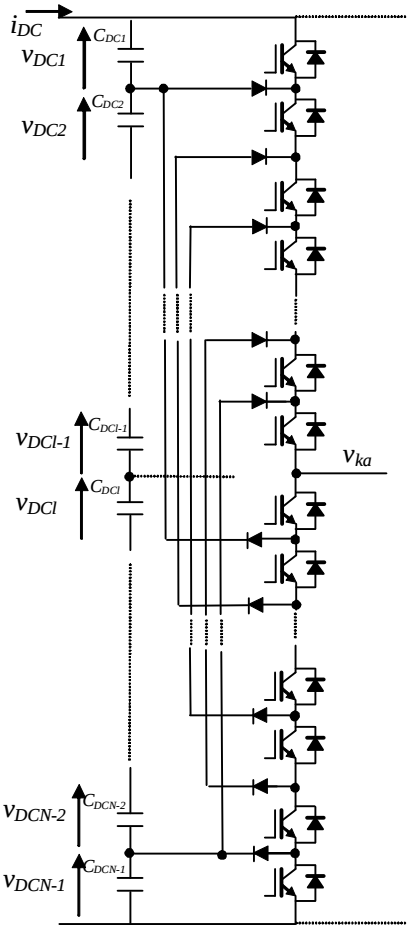


Fig.2.9: One-phase representation of N-Level-NPC VSI

$$
\begin{aligned}
v_{ka} &= \sum_{l=1}^{N-1} \frac{2S_{al} - (S_{bl} + S_{cl})}{3} v_{DCl} \\
v_{kb} &= \sum_{l=1}^{N-1} \frac{2S_{bl} - (S_{al} + S_{cl})}{3} v_{DCl} \\
v_{kc} &= \sum_{l=1}^{N-1} \frac{2S_{cl} - (S_{al} + S_{bl})}{3} v_{DCl}
\end{aligned}
\tag{2.12}
$$

Using (2.3), the system analytical model in the three-phase coordinates ***abc*** can be defined as follows:

$$
\begin{cases}
\dfrac{di_a}{dt} = -\dfrac{R}{L} i_a - \dfrac{1}{L} v_a + \dfrac{1}{L} \displaystyle\sum_{l=1}^{N-1} \dfrac{2S_{al} - (S_{bl} + S_{cl})}{3} v_{DCl} \\
\dfrac{di_b}{dt} = -\dfrac{R}{L} i_b - \dfrac{1}{L} v_b + \dfrac{1}{L} \displaystyle\sum_{l=1}^{N-1} \dfrac{2S_{bl} - (S_{al} + S_{cl})}{3} v_{DCl} \\
\dfrac{di_c}{dt} = -\dfrac{R}{L} i_c - \dfrac{1}{L} v_c + \dfrac{1}{L} \displaystyle\sum_{l=1}^{N-1} \dfrac{2S_{cl} - (S_{al} + S_{bl})}{3} v_{DCl} \\
C_{DC1} \dfrac{dv_{DC1}}{dt} = -(S_{a1} i_a + S_{b1} i_b + S_{c1} i_c) + i_{DC} \\
C_{DC2} \dfrac{dv_{DC2}}{dt} = -(S_{a2} i_a + S_{b2} i_b + S_{c2} i_c) + i_{DC} \\
.. \\
.. \\
C_{DCN-1} \dfrac{dv_{DCN-1}}{dt} = -(S_{aN-1} i_a + S_{bN-1} i_b + S_{cN-1} i_c) + i_{DC}
\end{cases}
\tag{2.13}
$$

The system representation in ***αβ*** and ***dq*** reference frames can be expressed as (2.14) and (2.15) respectively:

$$
\begin{cases}
\dfrac{di_a}{dt} = -\dfrac{R}{L} i_a - \dfrac{1}{L} v_a + \dfrac{1}{L} \displaystyle\sum_{l=1}^{N-1} v_{DCl} f_{la} \\
\dfrac{di_b}{dt} = -\dfrac{R}{L} i_b - \dfrac{1}{L} v_b + \dfrac{1}{L} \displaystyle\sum_{l=1}^{N-1} v_{DCl} f_{lb} \\
C_{DC1} \dfrac{dv_{DC1}}{dt} = -\dfrac{3}{2} (f_{1a} i_a + f_{1b} i_b) + i_{DC} \\
C_{DC2} \dfrac{dv_{DC2}}{dt} = -\dfrac{3}{2} (f_{2a} i_a + f_{2b} i_b) + i_{DC} \\
.. \\
C_{DCN-1} \dfrac{dv_{DCN-1}}{dt} = -\dfrac{3}{2} (f_{N-1a} i_a + f_{N-1b} i_b) + i_{DC}
\end{cases}
\tag{2.14}
$$

$$\begin{cases} \dfrac{di_d}{dt} = -\dfrac{R}{L} i_d - w i_q - \dfrac{1}{L} v_q + \dfrac{1}{L} \sum_{l=1}^{N-1} v_{DCl} f_{N-1d} \\ \dfrac{di_q}{dt} = -\dfrac{R}{L} i_q + w i_d - \dfrac{1}{L} v_q + \dfrac{1}{L} \sum_{l=1}^{N-1} v_{DCl} f_{N-1q} \\ C_{DC1} \dfrac{dv_{DC1}}{dt} = -\left(f_{1d} i_d + f_{1q} i_q \right) + i_{DC} \\ C_{DC2} \dfrac{dv_{DC2}}{dt} = -\left(f_{2d} i_d + f_{2q} i_q \right) + i_{DC} \\ .. \\ C_{DCN-1} \dfrac{dv_{DCN-1}}{dt} = -\left(f_{N-1d} i_d + f_{N-1q} i_q \right) + i_{DC} \end{cases} \tag{2.15}$$

Where the appropriate switching states are:

$$f_{la} = \frac{2S_{al} - (S_{bl} + S_{cl})}{3}$$

$$f_{lb} = \frac{1}{\sqrt{3}} (S_{bl} - S_{cl})$$

$$\text{where } l = 1..\,\mathrm{N}-1$$

$$f_{ld} = f_{la} \cos(wt) + f_{lb} \sin(wt)$$

$$f_{lq} = f_{lb} \cos(wt) - f_{la} \sin(wt)$$

whith $l = 1..\,\mathrm{N}-1$.

2.3. Space Vector Modulation

The switching-control signal (turn-on/turn-off) of modern power electronics converters are usually generated by Pulse Wide Modulation (PWM) techniques, which have become the basis of energy processing. Among the available PWM techniques, the space vector modulation has become very popular in many applications due to its simplicity. It is based on the spatial projection of the voltages of the three phases of the converter which results in a simple geometrical system's description and facilitates the analysis of the switching operation. This way, different kinds of vector-based modulations have been designed for specific performances[30;32;43;65-67;67;68;68-73]. In this dissertation the most popular vector-based modulators for MV operation conditions have been assumed. Thus, the main characteristics, operation range and some switching frequency performance criteria have been discussed.

2.3.1. Space Vector – Pulse Wide Modulation (SV-PWM)

The SV-PWM is the most extended modulation technique utilized in three-phase two-level VSIs. It employs the space vector representation of the converter's voltages in order to generate a reference average voltage vector $n^{\mathbf{r}}_{k}{}^{*}$ in the AC-side. The space vector α-β surface is divided in six sectors of 60º [θ_1.. θ_6], see Fig.2.10. The required average voltage vector is obtained using the combination of the two nearest active vectors along with two null vectors. The voltage vectors' sequence must be chosen in such a way that only one leg of VSI can switch between two consecutive vectors. Fig.2.11 shows, for example, the voltage application sequences which can be employed in the first sector.

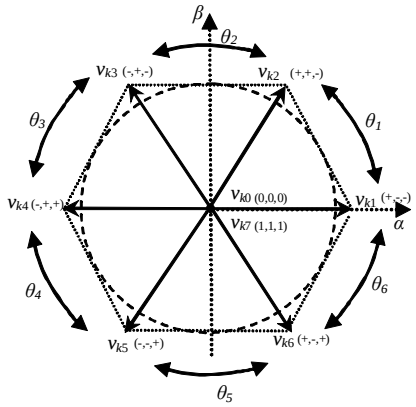
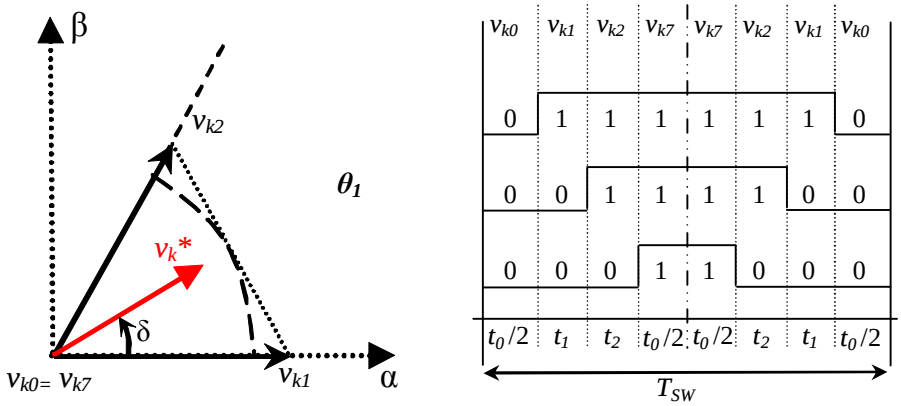


Fig.2.10: Set of available voltage-vectors on a three phase converter and mapping of the segments related to the line-voltage vector location under a SV-PWM



a) b)

Fig.2.11: Voltage vectors' sequence available in the first sector for SV-PWM: a) Graphical representation, b) Vectors application along a control period T_{SW}

As can be observed in Fig.2.11b, these vectors are applied in a symmetrical way in order to improve the steady-state operation using the minimum number of commutations. The application times are computed as follows.

$$\mathbf{v}_k^* \frac{T_{SW}}{2} = \mathbf{v}_{k1} t_1 + \mathbf{v}_{k2} t_2 + \mathbf{v}_{k0} t_0 \tag{2.16}$$

Where

$$\begin{aligned} v_{k1} &= \frac{2}{3} v_{DC} \\ \mathbf{v}_{k2} &= \frac{2}{3} v_{DC} \left(\frac{1}{2} + j \frac{\sqrt{3}}{2} \right) \\ \mathbf{v}_{k0} &= 0 \\ \mathbf{v}_k^* &= \left| \mathbf{v}_k^* \right| (\cos d + j \sin d) \end{aligned} \tag{2.17}$$

Having solved the equations concerned, the following times are obtained.

$$t_1 = \frac{3}{2v_{DC}\sqrt{3}}\left|\mathbf{v}_k^*\right| T_{SW} \sin\left(60^o - d\right)$$

$$t_2 = \frac{3}{2v_{DC}\sqrt{3}}\left|\mathbf{v}_k^*\right| T_{SW} \sin\left(d\right) \tag{2.18}$$

$$t_0 = \frac{T_{SW}}{2} - t_1 - t_2$$

If the line-voltage vector is in other sector, the control first translates the involved variables to the first sector, and then the same set of equations used for sector one can be exploited.

From these equations it is possible to deduce that the voltage vector will be maximum when t_0=0, operating across the hexagon showed in Fig.2.10. Therefore, the reference average voltage vector is usually limited in the module to $v_{DC}/\sqrt{3}$, which can be represented graphicaly as a circle inside the hexagon. The operation range of this kind of modulator offers the following converter's maximum linear line voltage rating

$$\frac{v_{kab(RMS)}}{v_{DC}} = 0.703 \tag{2.19}$$

In order to evaluate the switching frequency related to modulation techniques two performance criteria have been defined. The first one is the apparent switching frequency, i.e., the average switching frequency observed by the grid f_{Asw}. In this case, the SV-PWM is based on a symmetrical four voltage-vectors' sequence which implies two commutations per leg within a control period, see Fig.2.11b. Therefore, the apparent switching frequency can be computed (equation (2.20)) taking into account the total number of commutations (N_{SW}=6), the number of phases (N_F=3) and the symmetrical switching pattern consequence (S_{SW}=2). On the other hand, equation (2.21) shows maximum switching frequency which can be carried out by converter's switches f_{swMAX}. As can be derived, the average and maximum frequency will be the same when the SV-PWM technique is employed.

$$f_{Asw} = \frac{N_{\mathrm{SW}}}{\mathrm{N_F} S_{SW} T_{SW}} = \frac{1}{T_{SW}} \tag{2.20}$$

$$f_{swMAX} = f_{sw} = \frac{1}{T_{SW}} \tag{2.21}$$

2.3.2. Minimum Loss Vector – Pulse Wide Modulation (MLV-PWM)

The MLV-PWM or also so-called Discontinuous PWM was proposed in [74] and has been widely developed in literature by many authors [65;75;76]. In comparison with the SV-PWM, one of the three legs does not commute during the switching period, leading to a reduction of 33% on the converter's switching frequency. There are several kinds of MLV-PWMs and switching losses can be improved up to 50% becoming very interesting solutions to high power equipments. However, these reductions strongly depend on the power factor of the load and modulator design considerations. In this case, the line-voltage plane is divided in six sectors of 60º, [θ_1.. θ_6], which are also divided in two subsectors, [θ_{iA}.. θ_{iB}], see Fig.2.12. The reference average voltage vector $\boldsymbol{v_k}^*$ is obtained using the combination of two nearest active vectors and one null vector. Similarly to the previous modulation strategy, two symmetrical voltage vectors' sequences must be chosen. Fig.2.13 shows an example of space plane division and the voltage vectors' application sequence for the first sector.

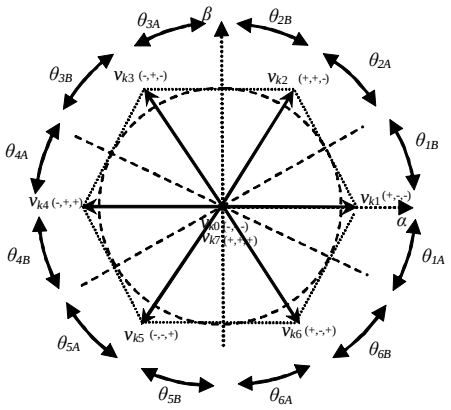


Fig.2.12: Set of available voltage-vectors on a three phase converter and mapping of the segments related to the line-voltage vector location under a MLV-PWM

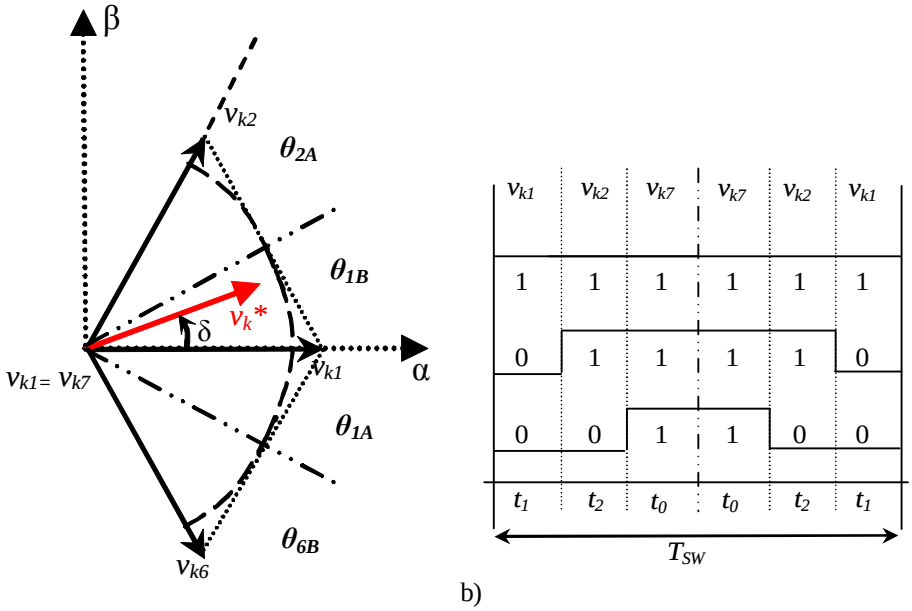


Fig.2.13: Voltage vectors' sequence available in the first sector under *B* sub-sector for MLV-PWM: a) Graphical representation, b) Vectors application along a control period T_{SW}

The voltage vectors' sequence is applied in a symmetrical way and the application times can be obtained using the same principle showed in 2.3.1. Therefore, equation (2.18) is also valid under MLV-PWM and the average vector is limited to $v_{DC}/\sqrt{3}$ in module. Furthermore, the maximum operation range of this kind of modulator is equal to equation (2.19). However, the MLV-PWM is based on four commutations per control period and the apparent switching frequency can be derived in equation (2.22), whereas the maximum switching frequency will correspond with the control frequency.

$$f_{Asw} = \frac{N_{SW}}{N_F S_{SW} T_{SW}} = \frac{2}{3T_{SW}} \tag{2.22}$$

$$f_{swMAX} = f_{sw} = \frac{1}{T_{SW}} \tag{2.23}$$

2.3.3. Nearest Three Vector – Space Vector Modulation (NTV-SVM)

The NTV-SVM is a widely employed vector-based modulation in multilevel converters[30;32;70;72;77;78]. This strategy combines the nearest two active vectors and one null vector in such a way that it generates the required voltage and keeps the voltage balance in DC-link capacitors. The space vector plane is divided in different sectors and regions where the combination of selected voltage vectors are the best to minimize the number of commutations, improve the power quality and minimize the generated electromagnetic interferences (EMIs). Fig.2.14 shows an example of the division of the line-voltage plane for a three-level NPC converter under six sectors of 60º [θ_1.. θ_6], which are also divided in four regions [R_{i1}.. R_{i4}], see Fig.2.15. The reference average voltage vector $\vec{n}_k^*$ is generated taking into account the sector and region, employing different combinations of large vectors $\vec{v}_{ki\_l}$, medium vectors $\vec{v}_{ki\_m}$, small vectors $\vec{v}_{ki\_s}$ and null vectors, $\{\vec{v}_{z0}, \vec{v}_{z1}, \vec{v}_{z2}\}$ [32;70;72;79-81]. Table 2.1 shows, for example, the voltage vectors' sequences which can be derived for the first sector fulfilling the DC-link capacitor's voltage balance requirements [79].

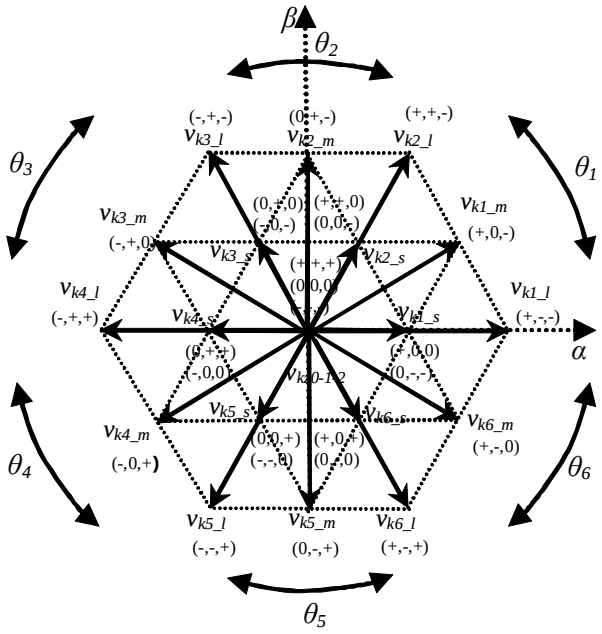


Fig.2.14: Set of available voltage-vectors on a three-level NPC converter and mapping of the segments related to the line-voltage vector location under a NTV-SVM

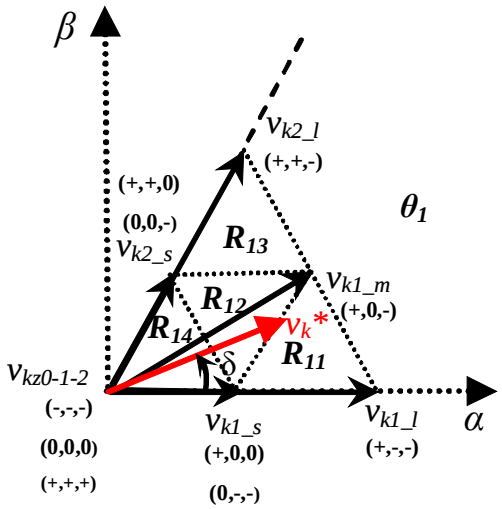


Fig.2.15: Graphical representation of voltage vectors' sequence available in the first sector for NTV-SVM

TABLE 2.1
SET OF AVAILABLE VOLTAGE VECTORS' SEQUENCES FOR THE FIRST SECTOR

REGION	DC-link capacitors' voltage balance requirements related to line current	Voltage vectors' sequence
1	$\overline{(v_{DC2} > v_{DC1}) \oplus (i_a < 0)}$	(0,-,-)-(+,-,-)-(+,0,-)
	$(v_{DC2} > v_{DC1}) \oplus (i_a < 0)$	(+,-,-)-(+,0,-)-(+,0,0)
2	$\overline{(v_{DC2} > v_{DC1}) \oplus (i_a < 0)} + (v_{DC2} > v_{DC1}) \oplus (i_c < 0)$	(0,-,-)-(0,0,-)-(+,0,-)
	$\overline{(v_{DC2} > v_{DC1}) \oplus (i_a < 0)} + \overline{(v_{DC2} > v_{DC1}) \oplus (i_c < 0)}$	(0,-,-)-(+,0,-)-(+,+,0)
	$(v_{DC2} > v_{DC1}) \oplus (i_a < 0) + (v_{DC2} > v_{DC1}) \oplus (i_c < 0)$	(0,0,-)-(+,0,-)-(+,0,0)
	$\overline{(v_{DC2} > v_{DC1}) \oplus (i_a < 0)} + \overline{(v_{DC2} > v_{DC1}) \oplus (i_c < 0)}$	(+,0,-)-(+,0,0)-(+,+,0)
3	$(v_{DC2} > v_{DC1}) \oplus (i_c < 0)$	(0,0,-)-(+,0,-)-(+,+,-)
	$\overline{(v_{DC2} > v_{DC1}) \oplus (i_c < 0)}$	(+,0,-)-(+,+,-)-(+,+,0)
4	$\overline{(v_{DC2} > v_{DC1}) \oplus (i_a < 0)} + \overline{(v_{DC2} > v_{DC1}) \oplus (i_c < 0)}$	(0,-,-)-(0,0,-)-(0,0,0) (0,0,-)-(0,-,-)-(-,-,-)
	$\overline{(v_{DC2} > v_{DC1}) \oplus (i_a < 0)} + (v_{DC2} > v_{DC1}) \oplus (i_c < 0)$	(0,-,-)-(0,0,0)-(+,+,0)
	$(v_{DC2} > v_{DC1}) \oplus (i_a < 0) + (v_{DC2} > v_{DC1}) \oplus (i_c < 0)$	(0,0,-)-(0,0,0)-(+,0,0)
	$\overline{(v_{DC2} > v_{DC1}) \oplus (i_a < 0)} + \overline{(v_{DC2} > v_{DC1}) \oplus (i_c < 0)}$	(+,0,0)-(+,+,0)-(+,+,+) (+,+,0)-(+,0,0)-(0,0,0)

In the same way as previous modulators, the voltage vectors' sequence is applied in a symmetrical way and application times can be obtained extending the method shown in 2.3.1 to a multi-region concept [70;79]. The maximum module of the average vector is limited in module to $v_{DC}/\sqrt{3}$, allowing an operation range described by equation (2.19). Furthermore, NTV-SVM is based on four conmutations per control period in such a way that the apparent switching frequency and the maximum switching frequency per semiconductor will be similar to those of the MLV-PWM strategy ((2.22) and (2.23)). However, it is necessary to emphasize that in a three level NPC converter the average frequency in each semiconductor within a semi-leg is different and mainly depends on the converter's operation point.

2.4. Design Considerations of Passive Components

The passive components have a strong effect on the size, efficiency and cost of VSI-based systems. This is the reason why they represent an interesting topic for designers and manufacturers. In literature there are many studies that discuss different methods of design [8;82-88].This section summarizes the main considerations to design the grid filter and the DC link capacitor in order to optimize a MV grid-connected installation.

The basic specifications and conditions of an MV converter example are shown in Table 2.2. The power rating and the line-to-line voltage are close to the commercial available MV units [1;17;20;21;21]. In the following analysis, it is assumed that the equipment operates as an inverter of the main source which supplies 2MW. The system is connected to a 2.3kV grid by means of an inductive filter. Both the Minimum Loss Vector and Nearest Three Vector SVM techniques are employed for 2L-VSI and 3L-NPC VSI respectively.

TABLE 2.2
SPECIFICATIONS OF GRID-CONNECTED MV VSI EXAMPLE

	Value [unit]	
Rated Power (S_k)	**2 [MVA] cos$q$=0.9(i)**	
Fundamental frequency *(fo)*	**50Hz**	
Rated line-to-line Voltage (RMS)	**2.3 [kV]**	
Grid Filter	**L-type**	
Topology	**2L-VSI**	**3L-NPC VSI**
Modulation	**(MLV-PWM)**	**(NTV-PWM)**

2.4.1. Grid Filter Design

As is well-known, the grid filter's reduces the current harmonics injected to the grid. The design of this device can be carried out in different ways; considering the voltage drop in the inductor, analysing the current ripple in high frequencies, identifying the harmonic spectrum generated by the converter and others [82;83;89;90]. Generally, the first and second methods are considered and the designer must find a good trade-off solution between them. The third technique could become an interesting method because it uses mathematical approaches of converter's voltage waveform spectra, showing a clear relation of harmonic components in front of the grid-connection standards. However, the resulting analytical expressions are not very friendly (they depend both on modulation technique and converter's topology) and usually simulation-based designs are utilized [13;68;91].

In this case an approach based on low and high frequency analyses has been developed. Thus, low frequency analysis will define the maximum inductor value (L_{MAX}) taking into account the voltage drop at fundamental frequency. On the other hand, high frequency analysis will define the minimum inductor value (L_{MIN}) taking into account current ripple values. The final value of the inductor will be selected between L_{MAX} and L_{MIN} observing which of them reflects the most important criteria. Other second criteria of design and final construction could be:

- Maximum current
- Tolerance
- Power losses in the filter resistance (defines the inductor-wind's section and material)

- Losses in the magnetic core (defines core's material)
- dV/dt during switching (defines inductor-wind's insulation)

Let us consider the per-phase diagram on Fig.2.16. The resistance of the inductor is assumed negligible for the design process.

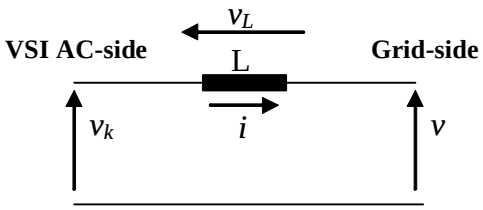


Fig.2.16: Per-phase grid-connected diagram with L-type filter

Equation (2.24), which uses RMS values of variables, shows the voltage drop in the grid filter at fundamental frequency

$$V_{L(LF)} = 2pf_0 LI \tag{2.24}$$

Thus, the maximum voltage drop $V_{Lmax(LF)}$ will imply a maximum inductor value L_{MAX}.

$$L_{MAX} = \frac{V_{L\max(LF)}}{2pf_0 I} \tag{2.25}$$

On the other hand, the current ripple is related to the converter's instantaneous voltage using the superposition method. Equation (2.26) shows the maximum instantaneous voltage step that can be deliver a N-level VSI, see Fig.2.17.

$$\Delta v_L = \frac{2}{3}\frac{V_{DC}}{(N-1)} \tag{2.26}$$

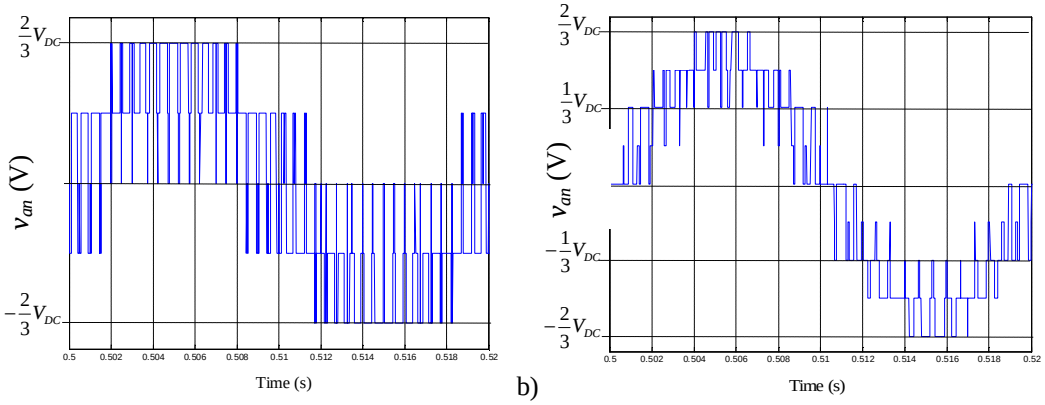


Fig.2.17: Instantaneous converter's per-phase voltage values related to neutral point of grid: a) 2L-VSI with MLV-PWM, b) 3L-NPC VSI with NTV-SVM

The per-phase voltage in an inductor v_L could be approached considering the relation between the voltage step variation v_{kn} in the inductance related to the instantaneous converter's per-phase voltage values an the average voltage drop $(v_k)_m$ toward it during the apparent switching period.

$$v_L \approx v_{kn} - (v_k)_m \tag{2.27}$$

The average voltage drop is related to the converter's static characteristic expression, see Fig.2.18. Equation (2.28) defines the static characteristic of N-level VSI which depends on the duty cycle (λ) and the converter's topology.

$$(v_k)_m = \frac{2V_{DC}}{3(N-1)} \cdot l \tag{2.28}$$

Nevertheless, if the apparent switching frequency is enough, the well-known inductor's voltage dynamic behavior can be approached as:

$$v_L = L\frac{di}{dt} \cong L\frac{\Delta i_{MAX}}{\Delta t} \tag{2.29}$$

Therefore, the current ripple can be approached considering a simple geometrical analysis, see Fig.2.18. Equation (2.30) shows the minimum inductor value expression taking into account the converter's topology, average switching frequency and duty cycle.

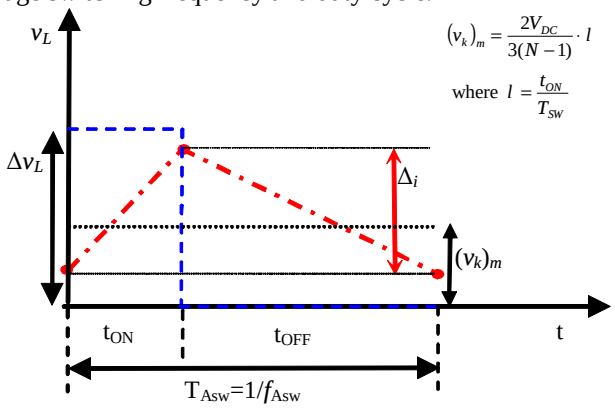
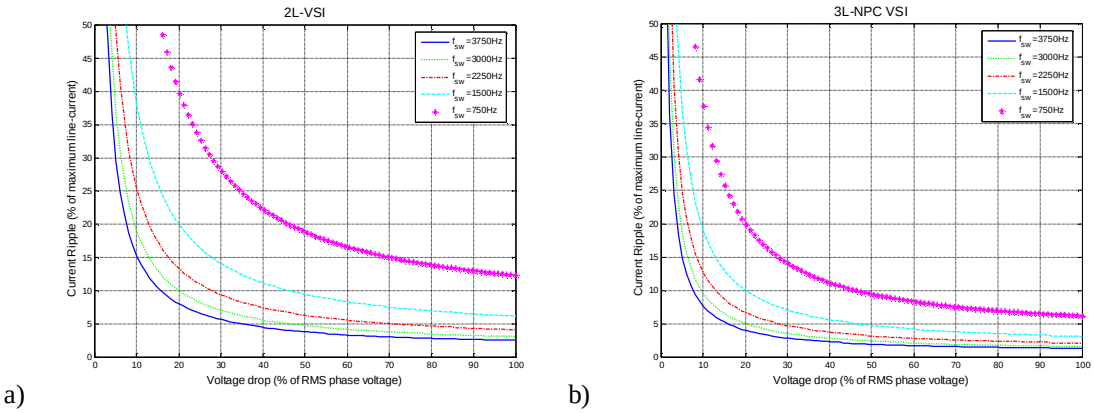


Fig.2.18: Current ripple approach during control period

$$\Delta i_{MAX} L_{MIN} = \frac{2V_{DC}(1-l)\,l}{3(N-1)f_{Asw}} \tag{2.30}$$

Finally, the selection of the inductor must be realized by the designer between L_{MAX} and L_{MIN} values. However, this method is rather ambiguous and allows different degrees of freedom which can be utilized in order to emphasize some design criteria against others. This work is focused on MV grid-connected converters. Because of this it is necessary to find a good trade-off solution between power quality and systems cost. The power quality is represented by current quality and the system's cost can be related to the voltage drop in the filter, which finally defines the converter's size. Though the maximum instantaneous current ripple is reached with a duty cycle of 0.5, this case has a little influence in the overall ripple behavior as it is only applied for a short time during each line-period. In fact, in sinusoidal-type evolution, the maximum duty-cycle is applied during the largest part of the period, so it can be considered as a good approximation to the overall ripple value. Fig.2.19 shows the relation between the current ripple and the voltage drop assuming a duty cycle of 0.9 under several switching frequencies and specifications shown in Table 2.1. The points of each graph are related to different inductors and the required minimum DC-voltage values.



a) b)

Fig.2.19: Current ripple related to voltage drop though L-type filter: a)2L-VSI, b)3L-NPC VSI

The 3L-NPC VSI, as expected, shows lower values of current ripple and voltage drop at a given switching frequency. On the other hand, it is necessary to consider that these kinds of MV converters must operate at switching frequencies below some kHz, assuring that power losses do not exceed the technological capability of semiconductors [17;21;92;93]. As a result, in the frame of this work, see Table 2.2, a technologically-possible frequency of 1.5kHz is considered. Fig.2.20 shows the current ripple and voltage drop under a switching frequency of 1.5kHz for both 2L-VSI and 3L-NPC VSI.

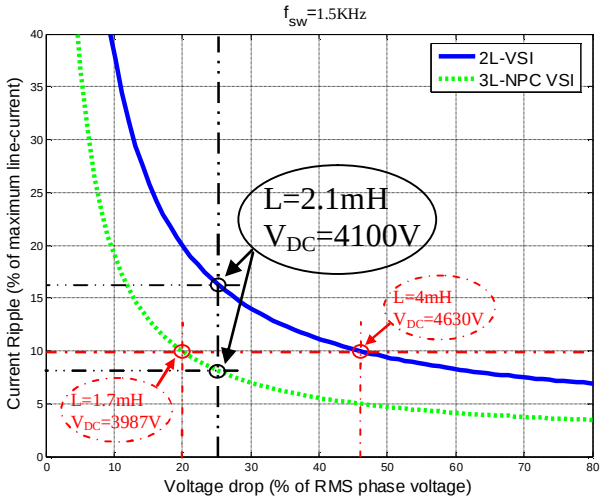


Fig.2.20: Current ripple related to voltage drop though L-type filter at 1.5kHz

Typically, a current ripple of 10% implies a THD of around 5% and fulfills the IEEE 519-1992 standard recommendation [17;92;93]. The 2L-VSI would require an extremely large inductor (4mH), which will results in a high voltage drop across it (47% of phase-voltage) and a high DC-link voltage (4630V). These results confirm other studies as [92], and it can be argued that the 2L-VSI with L-type filter is not a useful medium-voltage converter if high efficiency and a low THD are required. On the other hand, 3L-NPC VSI needs a smaller inductor (1.7mH) and DC-link voltage values (3987V) with a voltage drop through the filter of around 20%.

Finally, in other to compare the behavior of different converters with the same filter, an inductor of 2.1mH is chosen for both the 2L-VSI and 3L-VSI. Thus inductor generates a voltage drop of 25% and requires a DC-link voltage of 4100V, see Fig.2.20. Therefore, the 2L-VSI will not fulfill the IEEE 519-1992 recommendation (current ripple of around 16%), whereas the 3L-VSI will be within this standard with a THD below 5% (current ripple of around 8%).

2.4.2. DC-Link Capacitor Design

The DC-link capacitor has an important influence from the installation viewpoint because it stores the energy that is necessary in the system. Therefore, the design of this component will depend on the application and will usually have a significant effect on the weight, size and final cost [85-87;87;89;90]. This work is related to grid-connected VSIs which operate as inverters of a main source, supplying a power level to the grid under a given power factor. Thus, some energy criteria must be used for the design of the DC-link capacitor. Other second criteria of design and final selection could be considered as:

- The maximum voltage (mainly defines the technology)
- The peak to peak and RMS current values

Fig.2.21 shows a generic diagram (both 2LVSI and 3L-NPC VSI) of a DC-link between the main source and the converter's DC side. The voltage behavior on the capacitor depends on the DC current i_{DC} and VSI operation which has been defined as a current function i_f (2.31).

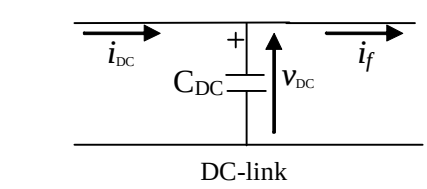


Fig.2.21: DC-link diagram

$$C_{DC}\frac{dv_{DC}}{dt} = i_{DC} - i_f \tag{2.31}$$

Considering the energy stored in the DC-link.

$$W = \frac{1}{2}C_{DC}v_{DC}^{\ 2} \tag{2.32}$$

Its variation can be expressed as:

$$\frac{dW}{dt} = C_{DC}v_{DC}\frac{dv_{DC}}{dt} \tag{2.33}$$

Taking into account this expression and multiplying (2.31) by v_{DC}, it is possible to get the well-known energy-balance equation.

$$\frac{dW}{dt} = P_{DC} - P_{if} \tag{2.34}$$

Where P_{DC} is the power delivered by the main source and with P_{if} is the power supplied to the grid by the VSI. Considering (2.33) and (2.34) and the maximum voltage variation at the DC-link Δv_{DC}, the capacitor's value can be approached to (2.35).

$$C_{DC} \geq \frac{\Delta P \cdot \Delta t}{\Delta v_{DC} \cdot v_{DC}} \tag{2.35}$$

where Δt is the delay time required by the control to adjust the outgoing power P_{if} to the new incoming power P_{DC}. This design criteria is usually employed in AC/DC/AC converters, also called back-to-back converters [53;86;90]. Other similar applications as rectifiers [94-96] only take into account the static behavior of the converter without considering the power variation in the DC-link. Anyway, typically a ripple from 1% to 10% of the DC-link voltage is assumed. On the other hand, the power variation and the delay-time needed by the DC-link control loop depend mainly on the characteristics of the main source. In the case of a wind-turbine application the semi-instantaneous power variations are limited to 10% of the rated power and it is supposed that the DC-link control loop is able to regulate it within two grid periods [6;89]. These consideration result on an acceptable capacitor value of 12mF assuming a 5% voltage ripple in the DC-link. Logically bigger capacitor values would give better output distortion results. However, the price and volume of the capacitors are also related to their ratting. Therefore, a compromise should be taken between a sufficient voltage ripple and a reasonable capacitor size.

2.5. Selection of Active Components

The medium/high power systems rated with the specifications listed in the Table 2.2, have been usually based on conventional technologies (Thyristors, GTOs, etc.). Today there are some studies that assure, under these power and voltage levels, improved features using HV-IGBTs [1;17;20;92]. The main advantages are a higher switching frequency, an easier driving due to the MOS-gate and improved cooling and insulation because of the fully isolated package. Some semiconductor manufactures as EUPEC classify their products depending on the field of applications. Fig.2.22, for instance, presents 6.5kV IGBT-based modules that usually are used for pumps, fans, compressors, and others medium-voltage drive applications [25].

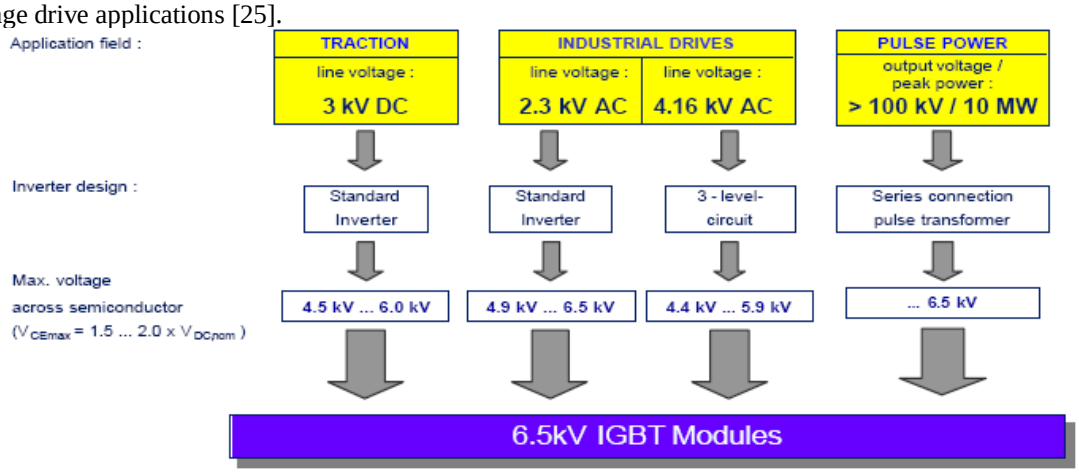


Fig.2.22: Application fields for 6.5kV modules [25]

However, it is not enough to select the IGBT modules based only on the rated current and voltage. It is also necessary to compute static and transient losses and temperature rises in the semiconductor modules. This field is out of the scope of this research where extensive iterative simulations must be carried out based on complex loss and thermal models [17;21;23;92;97;98]. Nevertheless, a good final design should take into account these considerations, selecting an optimal set of semiconductors.

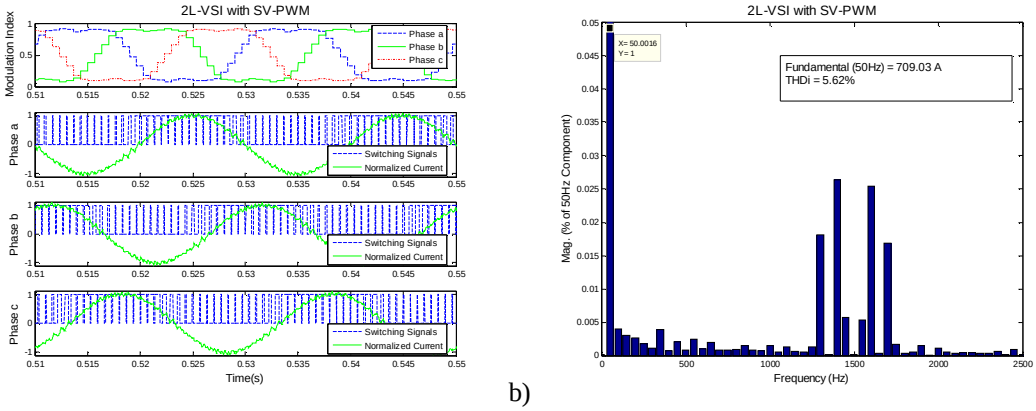
2.6. Simulation Results

In order to verify the design of the proposed MV grid-connected converter's, several simulations involving the 2L-VSI (with SV-PWM and MLV-PWM) and the 3L-NPC VSI (with NTV-SVM) have been carried out. The specifications and parameters of simulation results are summarized in Table 2.3.

TABLE 2.3
SPECIFICATIONS OF THE GRID-CONNECTED THREE-PHASE VSIs

	Value [unit]		
Rated Power (S_k)	**2 [MVA] cos$q$=0.9(i)**		
Fundamental frequency *(fo)*	**50Hz**		
Rated line-to-line Voltage (RMS)	**2.3 [kV]**		
L-type Filter	**2.1[mH]**		
DC-link	**12[mF] / 4100 [V]**		
Topology	**2L-VSI**	**2L-VSI**	**3L-NPC VSI**
Modulation	**(SV-PWM)**	**(MLV-PWM)**	**(NTV-PWM)**
Switching frequency	**f_{sw}=1500 [Hz]**	**f_{sw}=1500 [Hz]**	**f_{sw}=1500 [Hz]**

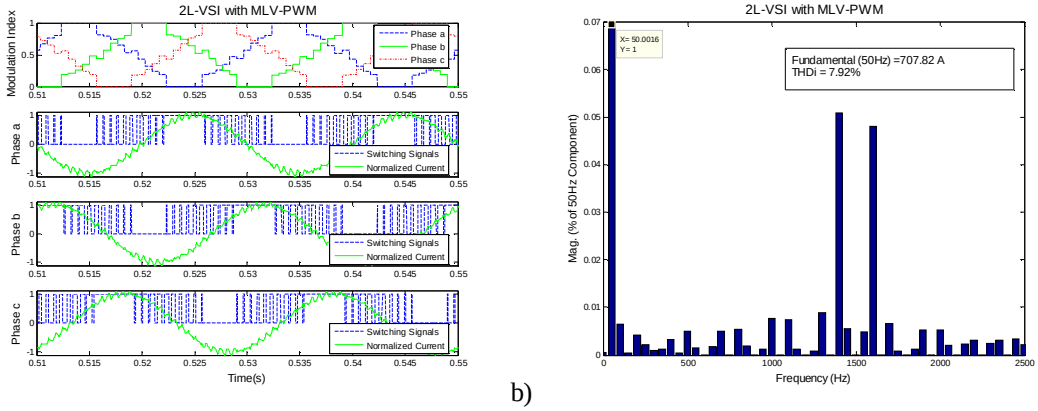
Fig.2.23a shows the modulation index and the line current along with the converter's switching signals for the 2L-VSI with SV-PWM under nominal operation conditions. The steady-state is evaluated analyzing the current THD. Fig.2.23b shows the harmonic spectrum which establishes a current THD of 5.62%, out of the Std. 519-1992 recommendation. It is an expected result considering the grid filter design of 2.4.1 which is not optimized for the 2L-VSI under the operation conditions established in Table 2.2.



a) b)

Fig.2.23: 2L-VSI with SV-PWM: a) Modulation index, phase switching signals and normalized line current, b) Current frequency spectrum

In fact, the 2L-VSI with MLV-PWM does not fulfill the standard recommendation, showing the worst current-quality (THDi=7.93%), see Fig.2.24. In this case, there is not any switching near the maximum of line-current, which is an interesting fact in relation to power-losses in high power applications. However, this improvement is closely related to current-spectrum deterioration.

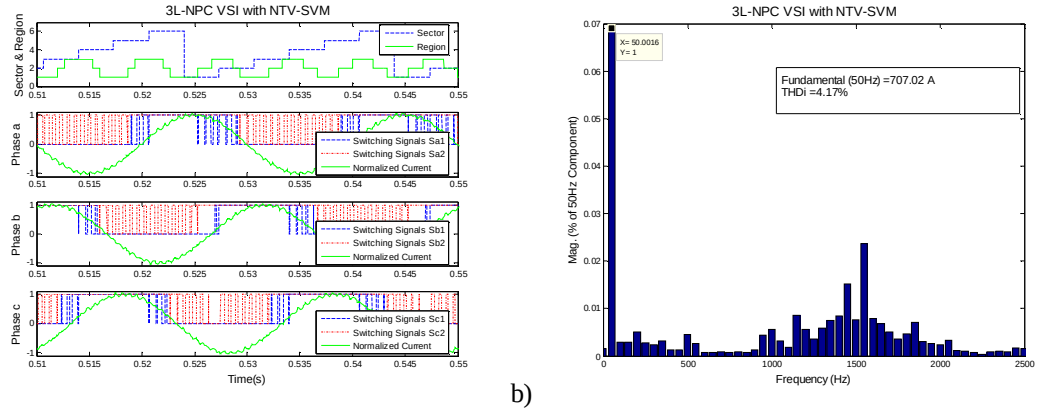


a) b)

Fig.2.24: 2L-VSI with MLV-PWM: a) Modulation index, phase switching signals and normalized line current, b) Current frequency spectrum

Finally, Fig.2.25 shows the simulation results of the 3L-NPC VSI operating with NTV-SVM strategy. The grid sector, region, per/phase switching signal, normalized current and frequency spectrum show in this figure an overview of the operation of the control. The steady-state operation matches with the the grid-filter design-considerations established in 2.4.1. The current THD below 5%, fulfills the Std. 519-1992 recommendation.

In order to evaluate the switching frequency behavior in the proposed configurations, the total number of commutations along a grid period has been computed, see Fig.2.26. Note that from this figure the apparent switching frequency can be straightforwardly derived if the total number of commutations during the grid period is considered in equation (2.20). Thus, 180 commutations during 20 ms results on an apparent frequency of 1500Hz, whereas 120 commutations will define an average frequency of around 1000Hz. MLV-PWM and NTV-SVM strategies then show a reduction of 33.33% in the switching frequency compared to SV-PWM. These results are expected because both strategies employ three voltage vectors per control period whereas SV-PWM is based on four voltage vectors.



a) b)

Fig.2.25: 3L-NPC VSI with NTV-SVM: a) Sector, Region, phase switching signals and normalized line current, b) Current frequency spectrum

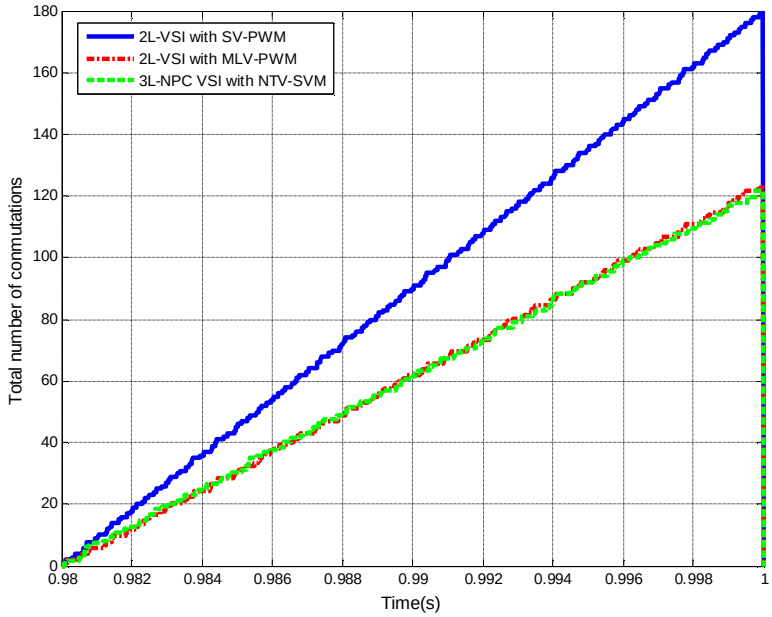
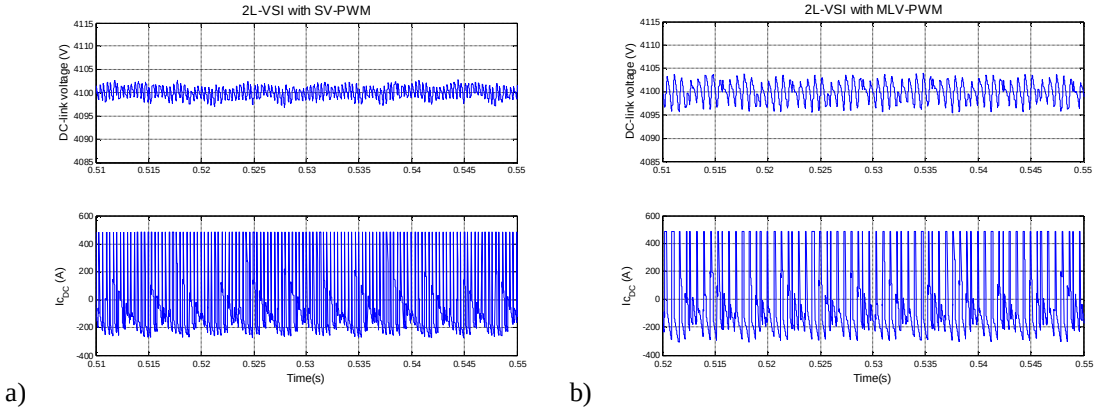


Fig.2.26: Total number of commutations along a grid period

The current and voltage ripple in the DC-link capacitors for the proposed configurations along two grid periods are shown in Fig.2.27 and Fig.2.28. These simulation have been carried out assuming the DC-link dynamic models of equation (2.4) and (2.9) under nominal operation conditions. In the 2L-VSI case, the SV-PWM strategy results on a denser DC-link current-ripple than MLV-PWM. Consequently, a smaller voltage ripple is generated at the DC-link. Thus, the SV-PWM-based configuration shows a DC-voltage ripple of around 0.05% with a RMS current of 273.49A through the capacitor, whereas the voltage ripple is near 0.1% and the RMS current is 274.84A when the MLV-PWM-type technique is utilized. In a similar way, Fig.2.28 shows the DC-voltage and current behavior related to 3L-NPC VSI with NTV-SVM. This configuration shows a DC-voltage ripple of 0.06% with a RMS current near to 273A through the capacitors which compose the DC-link. In addition, a characteristic perturbation of this kind of modulators at the typical frequency of 150Hz is identified.



a) b)

Fig.2.27: DC-link voltage and capacitor's current ripple: a) 2L-VSI with SV-PWM, b) 2L-VSI with MLV-PWM

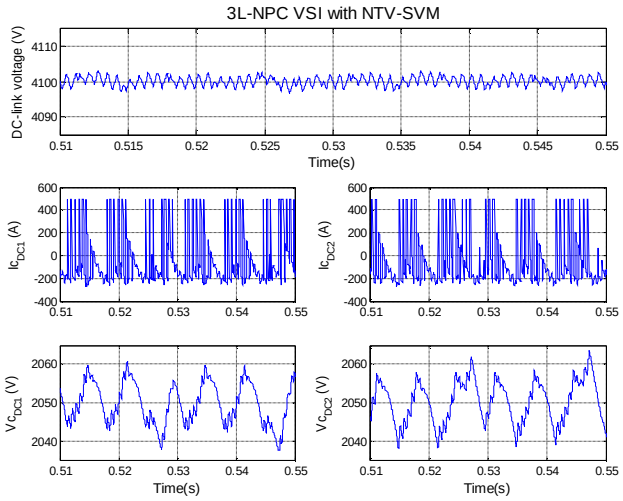


Fig.2.28: DC-link voltage and capacitors' current ripple and voltage in 3L- NPC VSI with NTV-SVM

2.7. Conclusions

In this chapter, some analysis and design considerations of grid-connected converters have been discussed. Concretely, the 2L-VSI and 3L-NPC VSI configurations with L-type filters have been studied, leading to a generalized development of N-level NPC VSI. Furthermore, some of the main features of the widely employed vector-based modulations have been shown, involving SV-PWM and MLV-PWM for the 2L-VSI and NTV-SVM for the 3L-NPC VSI. Moreover, passive components of MV grid-connected converters have been designed taking into account basic specifications and conditions which are close to the commercially available units. In fact, a grid-filter design approach using low and high frequency considerations has been developed and some energy criteria for DC-link capacitor design have been utilized.

The L-type filter for MV grid-connected applications has been selected due to its simplicity and reliability. Though it is a satisfactory choice for the 3L-NPC-VSI case, the 2L-VSI topology requires an extremely larger inductor in order to fulfill the standard IEEE 519-1992 recommendation. This high inductor value leads to a high voltage drop and consequently a higher DC-link voltage requirement. Therefore, the 2L-VSI with L-type filter is not a useful MV converter topology if high efficiency and low THD is required. One way to overcome this problem would be the choice of LC or LCL filters, which will be taken into account in future studies.

The DC-link capacitor design procedure is based on the knowledge of the energy exchanged between a wind-turbine and the grid, and has been carried out considering usual power variations, the maximum DC-link voltage ripple and the typical time of commonly used controls.

An optimum selection of active components of the proposed configurations requires extensive iterative simulations based on complex loss and thermal models which are out of the scope of this thesis. This research only deals with the state of the art provided by some manufacturers as EUPEC.

Finally, several simulations have verified the validity of the proposed converters for MV grid-connected operation conditions. They have been compared between using several indicators, as the current quality (by means of the THD), apparent switching frequency and DC link voltage ripple. It is possible to conclude that the 2L-VSI is not well behaved for MV operation with a simple inductive filter. On the other hand, the 3L-NPC VSI with NTV-SVM shows a very good steady-state performance and fulfills the connection requirements contained on the Std. 519-1992 recommendation. In spite of this, its basic configuration generates the well known 150Hz harmonic in the DC-link voltage.

Chapter 3

3. Power Control Strategies for Grid-connected VSI-based Systems

3.1. Introduction

Generally, VSI-based systems must provide a target active and/or reactive power to the line, and for this an appropriate power control strategy is required. As it has been shown in Chapter 1, although there are many strategies to control grid-connected converters, VOC-type indirect control is commonly employed. It has become a very popular control technique, developed widely in applications such as power generation, drives, power quality systems, and others [2;39;44;56;90;99-101]. On the other hand, DPC has been developed by many researches because it offers faster transients and robust behavior, employing directly active and reactive power tracking requirements [45;46;48;49;51;54;55;86;96].

This chapter evaluates both control methods and shows the main features and requirements under MV grid-connection operations. This way, VOC and DPC-based strategies for the 2L-VSI and 3L-NPC VSI have been developed in such a way that the steady-state and transient-state operation performances have been analyzed.

3.2. Voltage Oriented Control (VOC)

The first Chapter has introduced the basic block diagrams and performance indexes of VOC-type based controls, see Fig.1.5 and Fig.1.6. The VOC strategy is based on the knowledge of the position of the line-voltage vector and the relative spatial orientation of the current vector. Typically, grid-connected converters' control-structures are based on Park's transformation to a rotating *dq0* reference frame (aligned with the line-voltage) [2;39;101]. In fact, it is usually built by two cascaded control loops so that a fast inner loop controls the grid current and an external loop the DC-link voltage. In Fig.1.5, the power exchange control is carried out by means of current control, which must be tuned considering some design criteria. Therefore, in this section a line current control loop based on rotating reference frame will be developed in order to obtain a good transient behavior and an acceptable steady-state operation for both the 2L-VSI and 3L-NPC VSI.

3.2.1. Line Current Control Loop

It is necessary to take into account that the models which have been developed in Chapter 1 are not linear. In order to simplify the analysis and synthesis of the control loops, linear models are usually used. It is straightforward to derive the following continuous models from equation 2.6.

$$\begin{aligned} \hat{v}_{kd} &= R\hat{i}_d + L\frac{d\hat{i}_d}{dt} - wL\hat{i}_q + \hat{v}_d \\ \hat{v}_{kq} &= R\hat{i}_q + L\frac{d\hat{i}_q}{dt} + wL\hat{i}_d + \hat{v}_q \end{aligned} \tag{3.1}$$

Here $v_{kd\text{-}q}$ represents the converter's average-voltage-vector in a switching period and defines the VSI as a linear controlled continuous voltage source. The transfer-function type block description is shown in Fig.3.1.

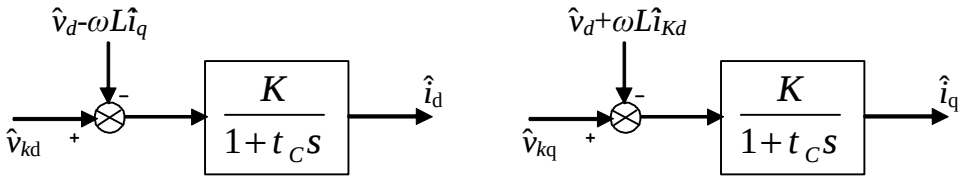


Fig.3.1: Block representation of current dynamic in dq reference frame

Thus, K is the DC gain and τ_C defines the time-constant of line-current dynamic behavior. The grid-voltage and cross-coupling effect can be considered as system's perturbations.

$$K = \frac{1}{R}$$
$$t_C = \frac{L}{R} \tag{3.2}$$

Fig.3.2 shows a generic block diagram for the line current control loop based on a PI controller, involving both d and q rotating components. The VSI is approached by a linear function where K_{VSI} defines the converter's gain, τ_{VSI} represents the switches' dead-time and the converter's time-constant includes the delay-time of the PWM technique (τ_{PWM}) and measurement-system's sample-delay (τ_s)[53;96;102]. Hence, the converter's gain can be assumed to be equal to K_{VSI}=1, and considering the statistical delay of PWM generation, we get τ_{PWM}=0.5T_{sw}. The dead-time is negligible in the case of ideal converters and the sample-delay time usually matches with the control period T_{sw}.

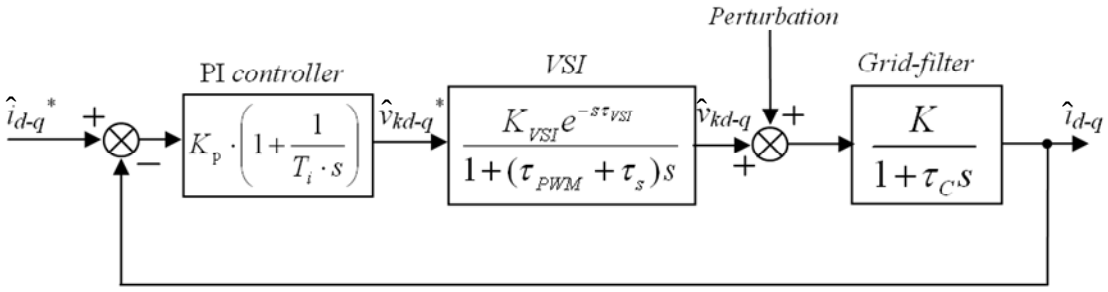


Fig.3.2: Block diagram of line current control loop approach

Considering that τ_C is the dominant time-constant the grid-filter model can be simplified as follows:

$$\frac{K}{1+t_C s} \cong \frac{K}{t_C s} \tag{3.3}$$

The open-loop and close-loop transfer functions of the system of Fig.3.2, neglecting the perturbation effect, are derived in equations (3.4) and (3.5).

$$F_{OL(S)} = \frac{K_p K(T_i s + 1)}{t_{DC} T_i s^2 \left(1 + \frac{3T_{SW}}{2} s\right)} \tag{3.4}$$

$$F_{CL(S)} = \frac{K_p K(T_i s + 1)}{t_C T_i s^2 \left(1 + \frac{3T_{SW}}{2} s\right) + K_p K(T_i s + 1)} \tag{3.5}$$

3.2.2. Controllers' Design Criteria

There are several methods and design criteria to select the parameters of PI controllers (K_p and T_i). Among these approaches; the Internal Model Control (IMC), Symmetry Optimum (SO) and Modulus Optimum (MO) are the best suited in order to make the controllers' design way straightforward [54;102;103]. In this case, SO-based considerations are applied in such a way that the maximum phase margin is obtained. Thus, the following conditions are established

$$T_i = r^2 (t_{PWM} + t_s) \tag{3.6}$$

$$W_0 = \frac{1}{r(t_{PWM} + t_s)} \tag{3.7}$$

Here ρ is a design parameter and W_0 is the desired system's wide-band under close-loop operation. The graphical representation approach of the SO method is shown in Fig.3.3.

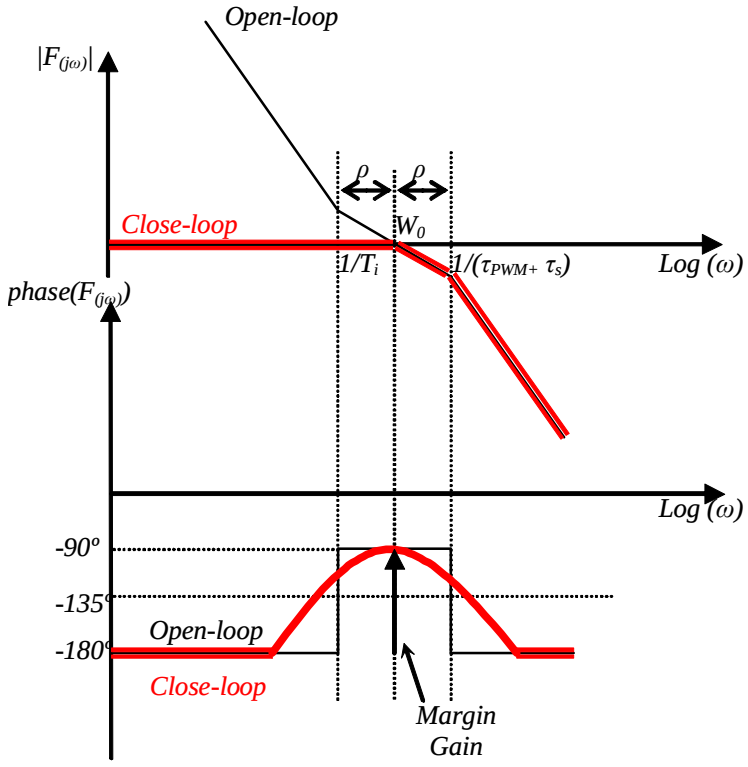


Fig.3.3: Graphical representation approach of Symmetric-Optimum method

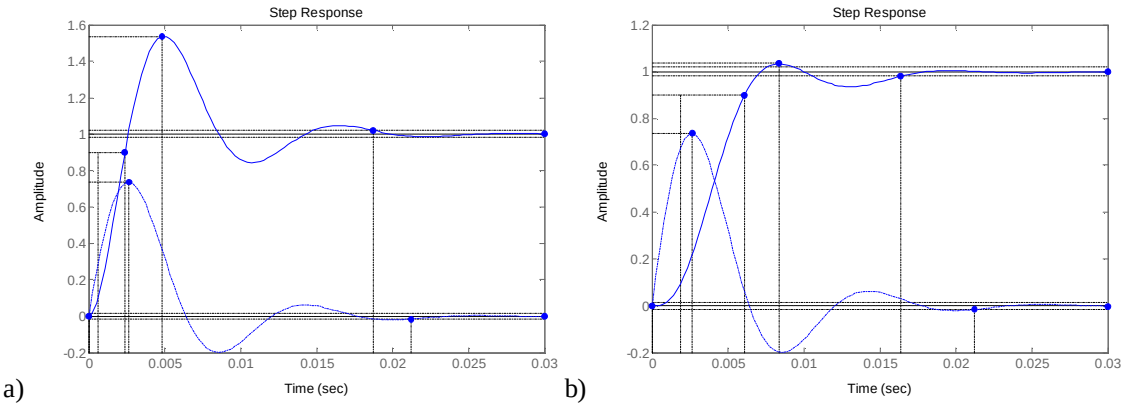
Therefore, the open-loop transfer function of equation (3.4) can be rewritten in the frequency domain ($s=j\omega$) if equation (3.6) is considered.

$$F_{OL(jw)} = -\frac{K_p K\left(r^2 \frac{3T_{sw}}{2} jw + 1\right)}{t_C r^2 \frac{3T_{sw}}{2} w^2 \left(1 + \frac{3T_{SW}}{2} jw\right)} \tag{3.8}$$

Taking into account that when ω is equal to W_0, the system's open-loop gain (in module) must be equal to unity ($|F_{OL(j\omega)}|=1$), the following expression for K_p is derived.

$$K_p = \frac{t_C}{\frac{3T_{sw}}{2} Kr} \tag{3.9}$$

Fig.3.4 shows the results of a parameter selection for current-control loop employing the specifications and conditions defined in Chapter 2 for the MV grid-connected 2L-VSI and 3L-NPC VSI. Concretely, Fig.3.4a shows a good (positive) transient response (solid line) during a step change on current reference value, with a setting time (within 2%) near 19ms and a rise time of 2ms. However, this design method shows a remarkable effect on the overshoot (57%) and a non negligible sensitivity to perturbations (dashed line) in transients. In order to reduce the overshoot, a previous filter, called a prefilter, is applied to the current reference [53;102;103], see Fig.3.5. Fig.3.4b shows a prefilter-based control system performance, leading to a fast transient response around 16ms with a rise time of 7ms, and reducing the overshoot substantially (3.46%). However, the prefilter has no influence on the behavior against perturbations and it is necessary to minimize its effects considering the cross-coupling relation between the *d* and *q* axes. Fig.3.6 shows the proposed VOC-type strategy involving the prefilters and the decoupled approach for current-control loop.



a) b)

Fig.3.4: Simulated current step response (solid) and perturbation reject (dashed) based on SO approach (ρ=1.7): a) without prefilter, b) with prefilter (τP=4(τPWM+ τs))

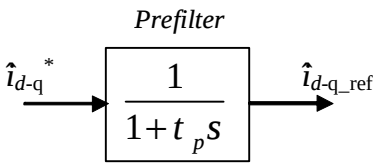


Fig.3.5: Block diagram of the current control loop previous filter (prefilter)

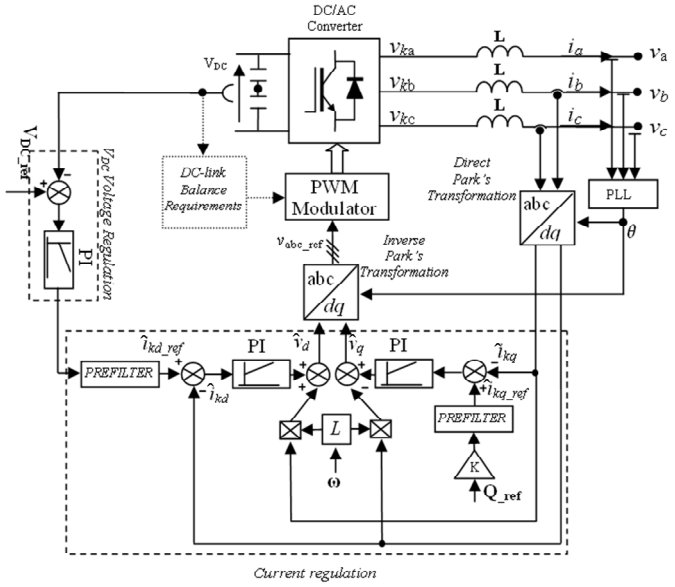


Fig.3.6: Block diagram of the proposed VOC in rotating reference frame

3.3. Direct Power Control (DPC)

Direct Power control (DPC) has become an interesting control strategy of grid-connected converters because it provides the maximum dynamic capability available in the system. This non-linear control strategy is defined as a direct control technique because it chooses the best suited converter's voltage vector without any modulation technique. The basic control structure of DPC has been shown in Fig.1.9 where two cascaded control loops are described; an internal active and reactive power regulation loop and an external control loop which establishes the DC-link voltage requirements. The inner loop evaluates directly active and reactive power tracking requirements, pushing the state of the system toward the reference values. This section will develop two DPC control strategies for the 2L-VSI and 3L-NPC VSI.

3.3.1. Power Control

The power control computes instantaneous active and reactive-power values. The definition of *instantaneous* power is still a source of controversy between researchers [104-111]. Among the theories that have been successively proposed over the last years, this work retains the "original" three-wire system's definition [110]. This way, instantaneous active and reactive power is defined as follows:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_a & v_b \\ -v_b & v_a \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \end{bmatrix} \tag{3.10}$$

Here $v_{\alpha\text{-}\beta}$ and $i_{\alpha\text{-}\beta}$ are the line voltage and current in static $\alpha\beta$ coordinates assuming power conservation in Clark's transformations. It is possible also to represent instantaneous active and reactive power using Park's transformations where $v_{d\text{-}q}$ and $i_{d\text{-}q}$, are the line voltage and current in the rotating dq reference frame. From the computation point of view, Clark's transformation uses simple linear relations whereas Park's transformation exploits trigonometric functions and requires to known the grid phase location, see *Appendix A*.

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} \hat{v}_d & \hat{v}_q \\ -\hat{v}_q & \hat{v}_d \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_d \\ \hat{i}_q \end{bmatrix} \tag{3.11}$$

The power control loop task continuously computes the instantaneous errors between the reference and the actual power values. These errors are evaluated by means of hysteresis controllers that establish the converter's switching state from a switching table, commonly called look-up table. Therefore, a correct implementation of DPC requires a fast estimation of the instantaneous power and an adequate look-up table.

This control strategy leads to variable switching frequency which depends mainly on the sampling time, the look-up table, the hysteresis wide-bands, the load parameters and the state of the system.

3.3.1.1. Grid Sector Selection and Hysteresis Controllers

One of the main design factors of DPC technique is the division of the grid-voltage space-plane in different sectors. In fact, it defines the look-up table where the best-suited voltage-vector available in the converter's AC-side is chosen. There are many possibilities of dividing the space-plane, but six-sector and twelve-sector-based solutions are commonly employed. In this dissertation a twelve-sector-based division has been retained for the 2L-VSI and 3L-NPC VSI configurations, see Fig.3.7. Note, that this distribution corresponds to the MLV-PWM technique (Chapter 2) where the space plane is divided in six sectors of 60º, [θ_1.. θ_6], which are also divided in two sub-sectors, [θ_{iA}.. θ_{iB}].

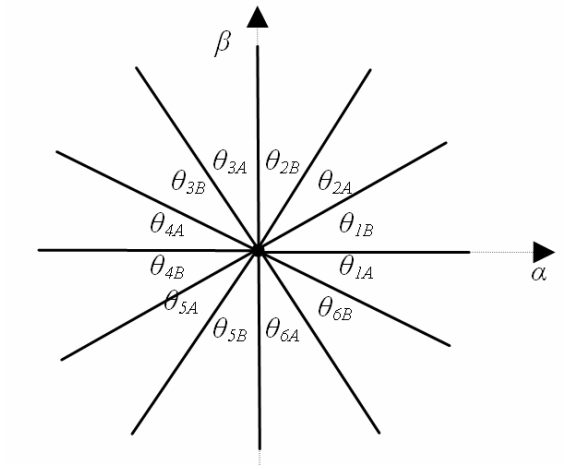


Fig.3.7: Sector selection for DPC

On the other hand, the type of hysteresis controllers has also an important effect on the conversion performance, i.e., in the apparent switching frequency, the resulting current spectrum and the power losses. The basic DPC structure usually exploits two-level hysteresis comparators, yet some interesting work has been carried out which proposes different combinations of two and three-level hysteresis controllers [43;48;49;112]. Generally, they establish a wide-band *H* round the active and the reactive power references in such a way that steady-state error can be limited. Fig.3.8 shows the two-level hysteresis comparators used in this dissertation. The controllers' laws are described in (3.12) and (3.13).

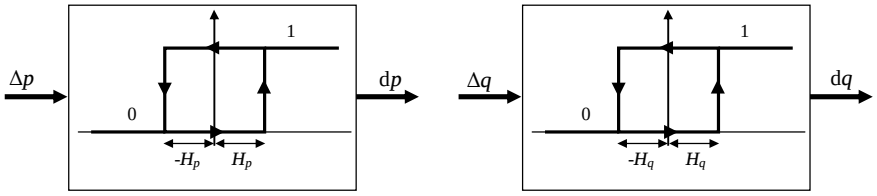


Fig.3.8: Two level hysteresis controllers

$$\begin{cases} \text{if } \Delta p > H_p \text{ then } \mathrm{d}p = 1 \\ \text{if } -H_d < \Delta p < H_d \text{ and } \dfrac{\mathrm{d}\Delta p}{dt} > 0 \text{ then } \mathrm{d}p = 0 \\ \text{if } -H_d < \Delta p < H_d \text{ and } \dfrac{\mathrm{d}\Delta p}{dt} < 0 \text{ then } \mathrm{d}p = 1 \\ \text{if } \Delta p < -H_p \text{ then } \mathrm{d}p = 0 \end{cases} \tag{3.12}$$

where $\Delta p = P\_ref - p$

$$\begin{cases} \text{if } \Delta q > H_q \text{ then } \mathrm{d}q = 1 \\ \text{if } -H_q < \Delta q < H_q \text{ and } \dfrac{\mathrm{d}\Delta q}{dt} > 0 \text{ then } \mathrm{d}q = 0 \\ \text{if } -H_q < \Delta q < H_q \text{ and } \dfrac{\mathrm{d}\Delta q}{dt} < 0 \text{ then } \mathrm{d}q = 1 \\ \text{if } \Delta q < -H_q \text{ then } \mathrm{d}q = 0 \end{cases} \tag{3.13}$$

where $\Delta q = Q\_ref - q$

3.3.1.2. Active and Reactive Power Time-derivatives

The instantaneous active and reactive-power time-derivatives establish the trend of the controlled variables, which is the key step of the construction of the look-up table. It is possible to predict the power behavior knowing the instantaneous variations of the active and reactive powers, which can be expressed as:

$$\begin{aligned} \frac{dP}{dt} &= v_a \frac{di_a}{dt} + i_a \frac{dv_a}{dt} + v_b \frac{di_b}{dt} + i_b \frac{dv_b}{dt} \\ \frac{dQ}{dt} &= v_b \frac{di_a}{dt} + i_a \frac{dv_b}{dt} - v_a \frac{di_b}{dt} - i_b \frac{dv_a}{dt} \end{aligned} \tag{3.14}$$

Equation (3.15) shows the per-phase dynamic behavior of a VSI with an inductive filter (Fig.3.9), with v_K the converter's voltage, v the line-voltage and i the line-current vectors.

$$v_K = R\, i + L \frac{di}{dt} + v \tag{3.15}$$

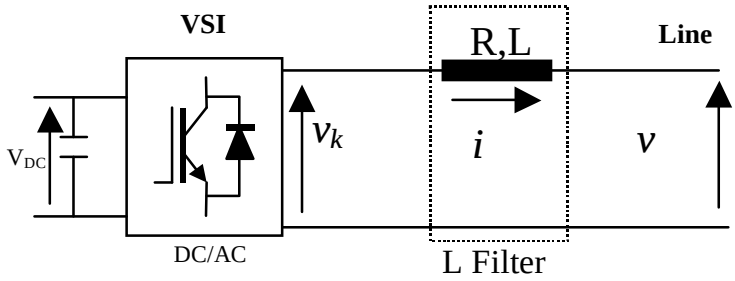


Fig.3.9: One-phase model of a line-connected VSI

Neglecting the influence of the resistances of inductive elements and using Clark's transformation, the instantaneous current behavior law under static coordinates is derived (3.16).

$$\begin{aligned} \frac{di_a}{dt} &\cong \frac{1}{L}\left(v_{Ka} - v_a\right) \\ \frac{di_b}{dt} &\cong \frac{1}{L}\left(v_{Kb} - v_b\right) \end{aligned} \tag{3.16}$$

The line-voltage variation is also required in (3.14). Considering a non-perturbed line:

$$\begin{aligned} v_a &= V_S \sin(wt) \\ v_b &= -V_S \cos(wt) \end{aligned} \tag{3.17}$$

Next instantaneous line-voltage variation law is obtained:

$$\begin{aligned} \frac{dv_a}{dt} &= V_S\, w \cos(wt) = -w\ v_b \\ \frac{dv_b}{dt} &= V_S\, w \sin(wt) = w\ v_a \end{aligned} \tag{3.18}$$

and replacing (3.16) and (3.18) in (3.14) it is possible to get the functions describing the instantaneous active and reactive-power time-derivatives.

$$\begin{aligned} \frac{dP}{dt} &= v_a\left(\frac{1}{L}\left(v_{Ka} - v_a\right) + w\ i_b\right) + v_b\left(\frac{1}{L}\left(v_{Kb} - v_b\right) - w\ i_a\right) \\ \frac{dQ}{dt} &= v_a\left(w\ i_a - \frac{1}{L}\left(v_{Kb} - v_b\right)\right) + v_b\left(\frac{1}{L}\left(v_{Ka} - v_a\right) + w\ i_b\right) \end{aligned} \tag{3.19}$$

The power time-derivative values depend on the grid variables, filter inductors and on the converter's switching state. Fig.3.10 (Fig.3.11) shows, under unity-power-factor and steady-state operation, the behavior of different active and reactive-power time-derivatives, related to different converter's voltage-vectors in the 2L-VSI (3L-NPC VSI) case.

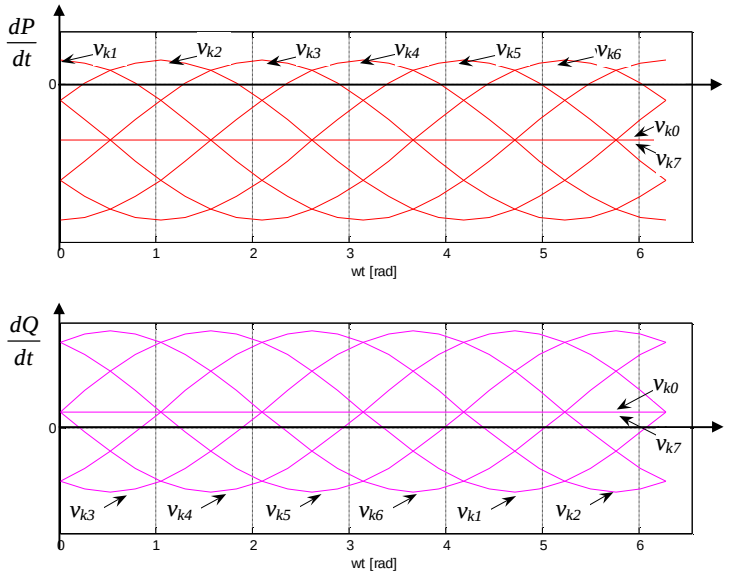


Fig.3.10: 2L-VSI: Active and reactive-power time-derivative behaviors under unity-power-factor steady-state operation

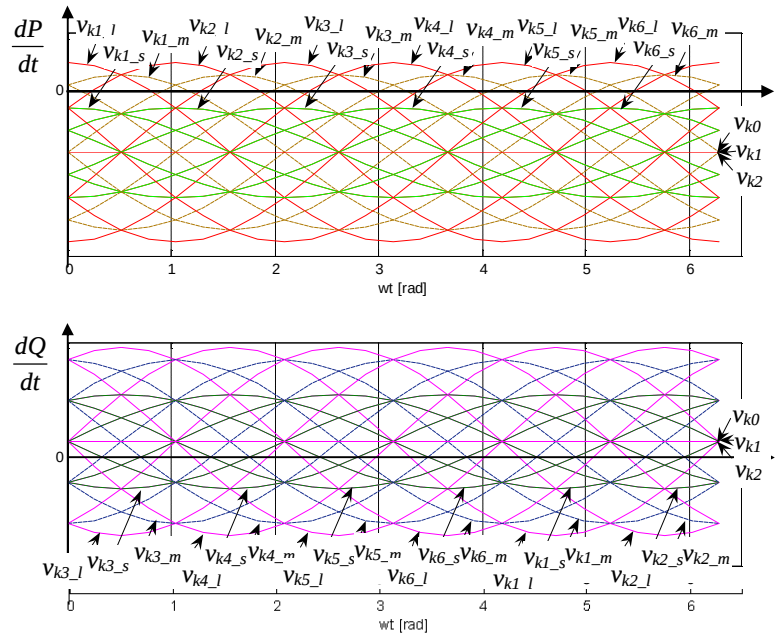


Fig.3.11: 3L-NPC VSI: Active and reactive-power time-derivative behaviors under unity-power-factor steady-state operation

3.3.2. Look-up Table Design

Fig.3.12 shows the time-derivative values under sector 2 for the 2LVSI case. It can be seen that the application of v_{k0}, v_{k7}, v_{k4}, v_{k5} or v_{k6} voltage-vectors implies a negative time-derivative of the active power. This way, if any of these vectors is applied, the active power tends to decrease. On the other hand, the use of v_{k2} leads to a positive time-derivative which will increase the active power. Furthermore, v_{k1} or v_{k3} can induce both positive and negative time-derivatives depending on the part of the sub-sector where they are used. The same procedure can be applied for the analysis of the reactive power behavior. Fig.3.13 shows the active and reactive-power time-derivatives for the 3L-NPC VSI case.

Table 3.1 and Table 3.2 show an example of look-up tables for the two proposed VSI configurations. In the 3L-NPC VSI case, different voltage vectors define similar time-derivative behaviors, allowing a redundancy in the selection of the switching-vectors. This redundancy can be employed under different control criteria, becoming the DC link balance the most popular. In fact, a combination of two different voltage-vectors in a sector is proposed, see Table 3.2 and Fig.3.13. The selection of each voltage-vector will depend on the 3L-NPC converter's neutral-point-voltage error, trying to minimize it. Fig.3.14 shows the proposed DPC-type strategy involving a DC-link balance for the 3L-NPC VSI.

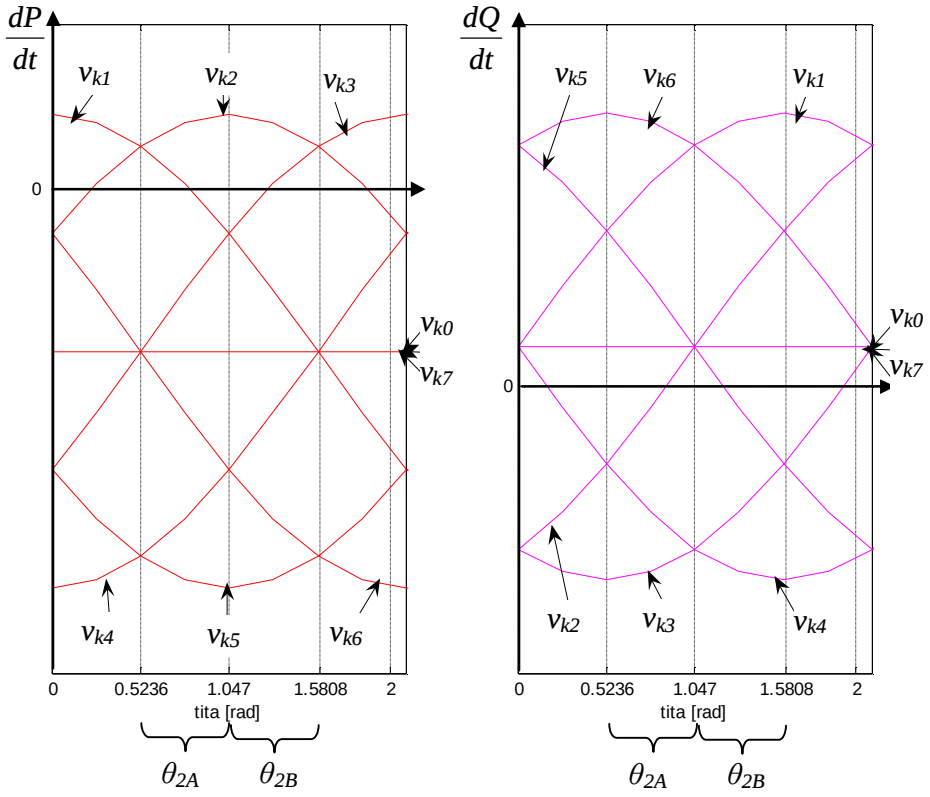


Fig.3.12: 2L-VSI: Active and reactive power time-derivative behaviors in sector 2

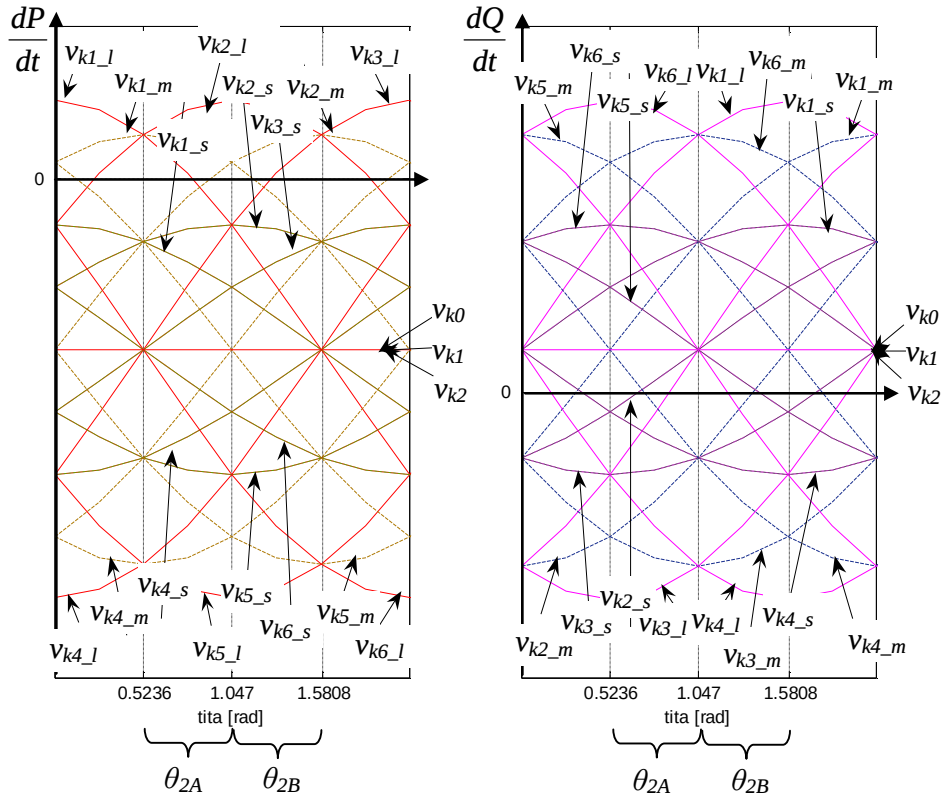


Fig.3.13: 3L-NPC VSI: Active and reactive power time-derivative behaviors in sector 2

TABLE 3.1
LOOL-UP TABLE OF 2L-VSI

dp	dq	θ_{1A}	θ_{1B}	θ_{2A}	θ_{2B}	θ_{3A}	θ_{3B}	θ_{4A}	θ_{4B}	Θ_{5A}	θ_{5B}	θ_{6A}	θ_{6B}
1	**1**	v_{k6}	v_{k1}	v_{k1}	v_{k2}	v_{k2}	v_{k3}	v_{k3}	v_{k4}	v_{k4}	v_{k5}	v_{k5}	v_{k6}
1	**0**	v_{k1}	v_{k2}	v_{k2}	v_{k3}	v_{k3}	v_{k4}	v_{k4}	v_{k5}	v_{k5}	v_{k6}	v_{k6}	v_{k1}
0	**1**	v_{k0}	v_{k0}	v_{k7}	v_{k7}	v_{k0}	v_{k0}	v_{k7}	v_{k7}	v_{k0}	v_{k0}	v_{k7}	v_{k7}
0	**0**	v_{k2}	v_{k3}	v_{k3}	v_{k4}	v_{k4}	v_{k5}	v_{k5}	v_{k6}	v_{k6}	v_{k1}	v_{k1}	v_{k2}

TABLE 3.2
LOOL-UP TABLE OF 3L-NPC VSI

dp	dq	θ_{1A}	θ_{1B}	θ_{2A}	θ_{2B}	θ_{3A}	θ_{3B}	θ_{4A}	θ_{4B}	θ_{5A}	θ_{5B}	θ_{6A}	θ_{6B}
1	**1**	v_{k6_m}	v_{k1_l}	v_{k1_m}	v_{k2_l}	v_{k2_m}	v_{k3_l}	v_{k3_m}	v_{k4_l}	v_{k4_m}	v_{k5_l}	v_{k5_m}	v_{k6_l}
		v_{k6_l}	v_{k1_m}	v_{k1_l}	v_{k2_m}	v_{k2_l}	v_{k3_m}	v_{k3_l}	v_{k4_m}	v_{k4_l}	v_{k5_m}	v_{k5_l}	v_{k6_m}
1	**0**	v_{k1_l}	v_{k2_m}	v_{k2_l}	v_{k3_m}	v_{k3_l}	v_{k4_m}	v_{k4_l}	v_{k5_m}	v_{k5_l}	v_{k6_m}	v_{k6_l}	v_{k1_m}
		v_{k1_m}	$v_{k2\_}$	v_{k2_m}	v_{k3_l}	v_{k3_m}	v_{k4_l}	v_{k4_m}	v_{k5_l}	v_{k5_m}	v_{k6_l}	v_{k6_m}	v_{k1_l}
0	**1**	v_{k6_s}	v_{k1_s}	v_{k1_s}	v_{k2_s}	v_{k2_s}	v_{k3_s}	v_{k3_s}	v_{k4_s}	v_{k4_s}	v_{k5_s}	v_{k5_s}	v_{k6_s}
0	**0**	v_{k2_s}	v_{k3_s}	v_{k3_s}	v_{k4_s}	v_{k4_s}	v_{k5_s}	v_{k5_s}	v_{k6_s}	v_{k6_s}	v_{k1_s}	v_{k1_s}	v_{k2_s}

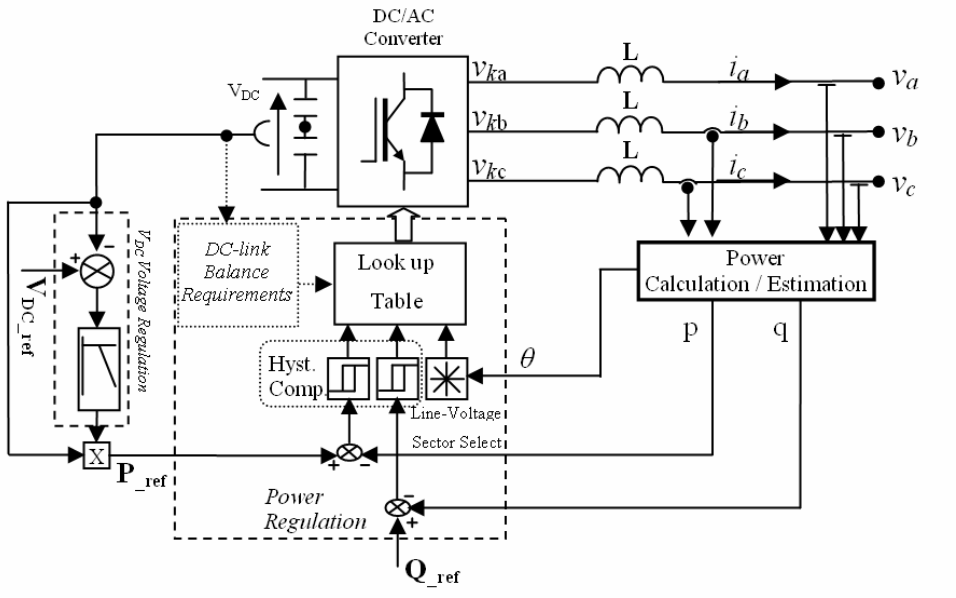


Fig.3.14: Block diagram of proposed DPC

3.4. Simulation Results

Simulations of the proposed control algorithms have been carried out with the aim to evaluate their behavior for MV grid-connected applications. Specifications described in Chapter 2 (Table 2.3) have been considered and steady-state and transient operation performances of the 2L-VSI and 3L-NPC VSI configurations have been analyzed. The steady-state is evaluated by means of current THD measurements (THD_i), active and reactive power ripple values (ΔP, ΔQ) and some DC-link performance features as the voltage ripple and the RMS current across the capacitors (Δv_{DC}, $Ic_{DC(RMS)}$). In addition, the absolute error between the reference value and the actual fundamental component (50Hz) of line-current has been computed. On the other hand, the cross-coupling effect and the typical dynamic performance criterions as the setting time, rise time and overshoot are considered in the transient-state operation.

Table 3.3 summarizes the main features and requirements of the suggested control strategies. Thus, in order to develop a coherent comparative frame a given average switching frequency of 1kHz has been assumed. The VOC type strategies require a control & sampling frequency 1.5 times larger than the desired apparent switching frequency, whereas the DPC of a 2L or 3L-NPC VSIs needs a control & sampling frequency 5 or 6 times larger than the apparent switching frequency. This is the reason why the control & sampling frequency of the DPC of the 2L-VSI goes up to 6kHz in contrast to the 1.5kHz required by the VOC type MLV-PWM.

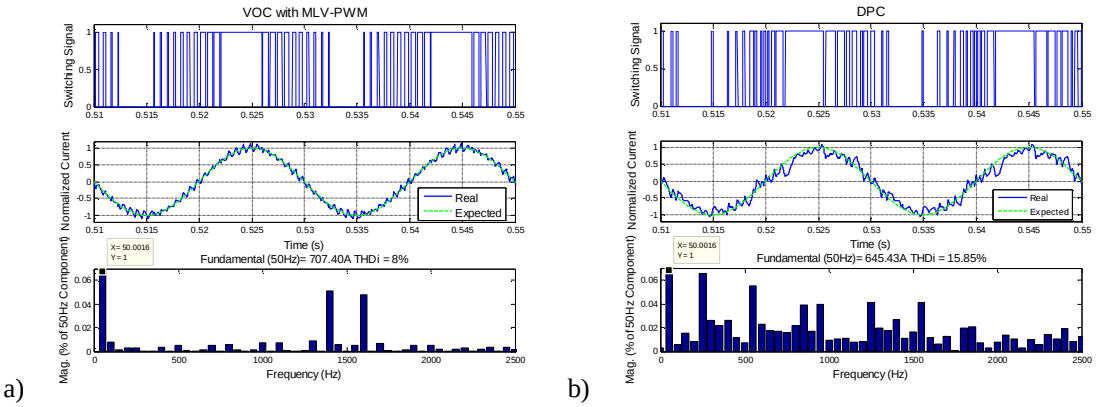
TABLE 3.3
MAIN CHARACTERISTICS OF CONTROL STRATEGIES

	Control Method	Apparent Switching Frequency	Control & Sampling Frequency
2L-VSI	VOC with MLV-PWM	1 [kHz]	1.5 [kHz]
	DPC	1 [kHz]	6 [kHz]
3L-NPC VSI	VOC with NTV-SVM	1 [kHz]	1.5 [kHz]
	DPC	1 [kHz]	5 [kHz]

3.4.1. Steady-state Performance

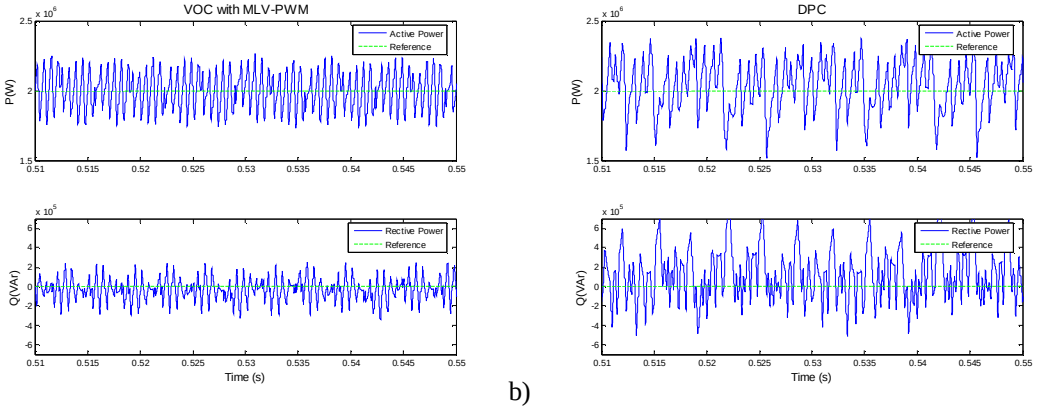
Fig.3.15 and Fig.3.16 show the per-phase switching signals, normalized line current, frequency spectrum and power performance for the 2L-VSI, using both the VOC-type control strategy with MLV-PWM and the DPC. As can be observed the VOC shows the best power quality (THD_i=8%) and the minimum power ripple (ΔP=12.73%, ΔQ=14.96%) with a bounded harmonic spectrum around the converter's switching frequency. The DPC leads to a dispersed harmonic spectrum with a large THD of around 16% with considerable power ripple values (ΔP=20%, ΔQ=31.83%). In spite of the fact that both strategies do not fulfill the IEEE Std 519-1992 recommendation, the VOC technique shows some advantages from the point of view of the grid filter design considerations and grid resonances prevention.

On the other hand, the VOC with MLV-PWM shows a small tracking error of around 0.36%, while the absolute tracking error reaches 9% in the DPC case. Furthermore, the voltage ripple in the DC-link capacitor is clearly smaller in the VOC (Δv_{DC}=0.14%) than the DPC strategy (Δv_{DC}=0.34%), see Fig.3.17. Nevertheless, the RMS current in the DC-link capacitors is lower in DPC ($Ic_{DC(RMS)}$=274.56 A) than in VOC ($Ic_{DC(RMS)}$=252.73A).



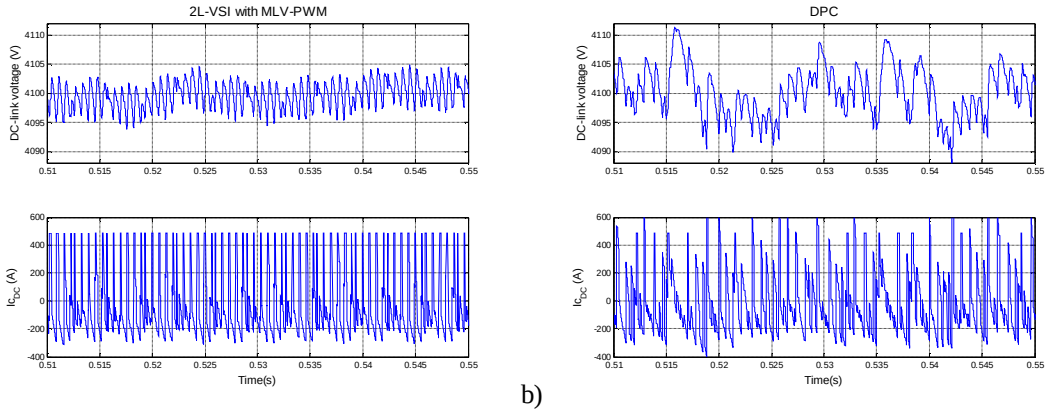
a) b)

Fig.3.15: 2L-VSI. Phase switching signals, normalized line current and frequency spectrum: a) VOC with MLV-PWM b) DPC



a) b)

Fig.3.16: 2L-VSI. Active and reactive power behaviors: a) VOC with MLV-PWM b) DPC



a) b)

Fig.3.17: 2L- VSI. DC-link voltage and capacitor's current ripple: a) VOC with NTV-SVM b) DPC

The average switching frequency is evaluated taking into account the total number of commutations in a grid period. Fig.3.18 describes the behavior of the switching occurrences on a 2L-VSI during a time frame from 0.98s to 1s. The VOC with MLV-PWM (solid-line) defines a linear trajectory which is characteristic in constant switching frequencies, whereas the DPC (dashed-line) shows an irregular performance. However, both control strategies employ the same number of commutations (around 120) along the grid period, establishing an average switching frequency of 1kHz.

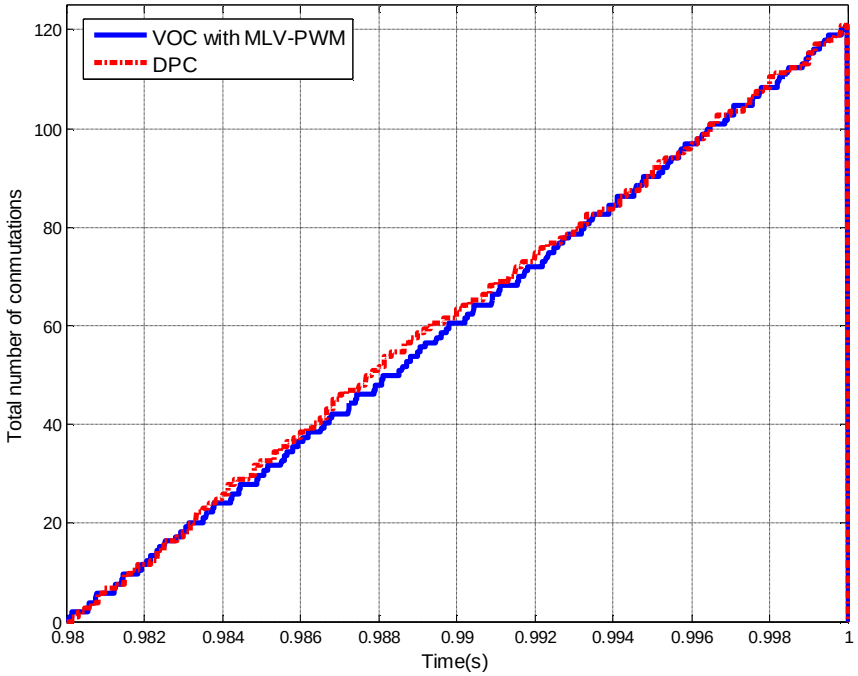
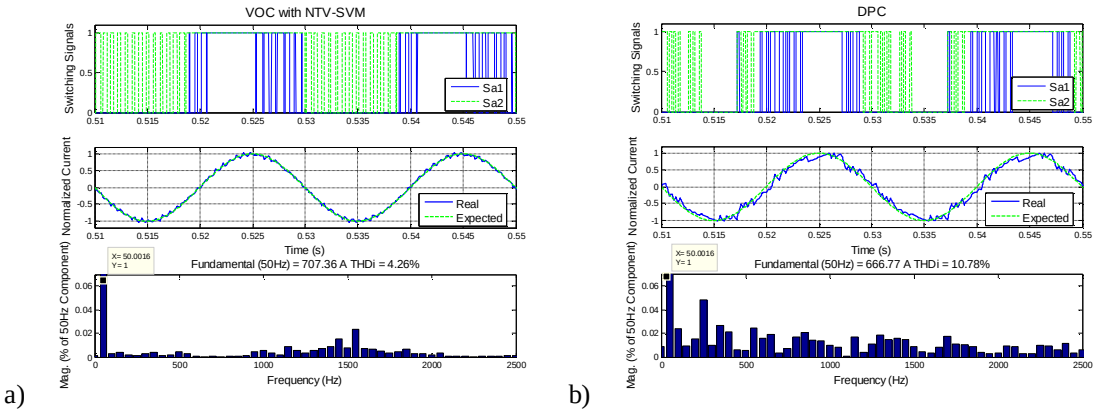


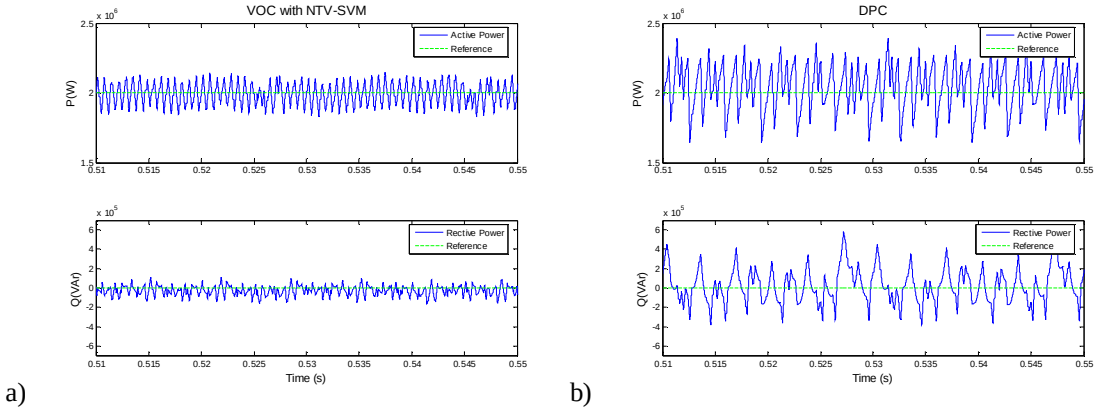
Fig.3.18: 2L-VSI. Total number of commutations in a grid period

The same two control strategies have been evaluated in the 3L-NPC VSI case. Fig.3.19 and Fig.3.20 show the simulated per-phase switching signals, normalized line current, frequency spectrum and power behaviors related to the proposed control algorithms. As can be derived, the VOC with NTV-SVM presents better results in steady-state power performance (ΔP=9.15%, ΔQ=8.27%) than in the DPC technique (ΔP=18.57%, ΔQ=23.60%). In fact, the current THD measurements are around 4.26% in the first case and 10.78% in the second case. This way, only VOC with NTV-SVM meets the IEEE Std. 519-1992 recommendation. As expected, the voltage ripple in the DC-link capacitors is clearly smaller in the VOC-based strategy (Δv_{DC}=0.11%) than in the DPC method (Δv_{DC}=0.25%), see Fig.3.21. The RMS current in the DC-link capacitors are around 272A and 244A respectively. Furthermore, the absolute tracking error is 0.37% in the VOC-type strategy whereas it is near 6% in the DPC.



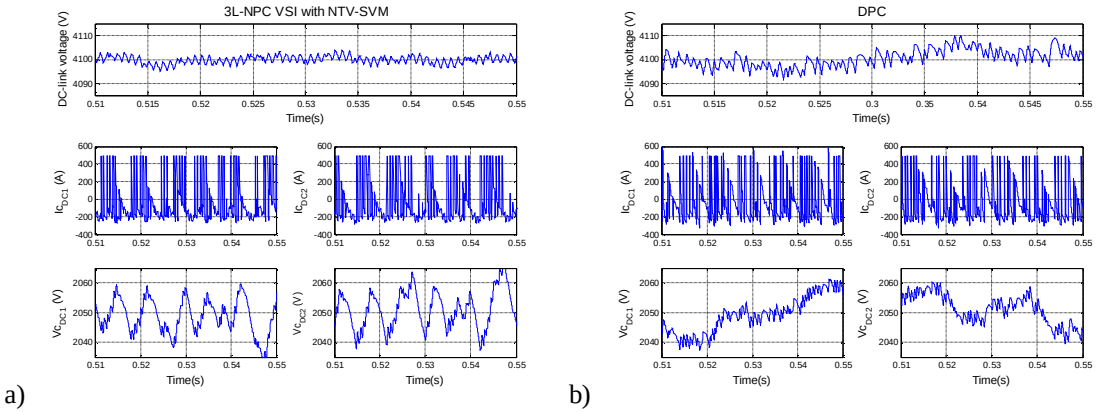
a) b)

Fig.3.19: 3L-NPC VSI. Phase switching signals, normalized line current and frequency spectrum: a) VOC with NTV-SVM b) DPC



a) b)

Fig.3.20: 3L-NPC VSI. Active and reactive power behaviors: a) VOC with NTV-SVM b) DPC



a) b)

Fig.3.21: 3L-NPC VSI. DC-link voltage and capacitor's current ripple: a) VOC with NTV-SVM b) DPC

Fig.3.22 shows the switching behavior of the 3L-NPC VSI with the two proposed control strategies in a grid period. The VOC with NTV-SVM (solid-line) operates at constant switching frequency and therefore it describes a linear trajectory. However, the DPC (dashed-line) is based on a variable switching pattern and it implies an irregular switching performance. In spite of this, both control strategies employ the same number of commutations along the grid period (near 120) and it could be said that they use the same average switching frequency of around 1kHz.

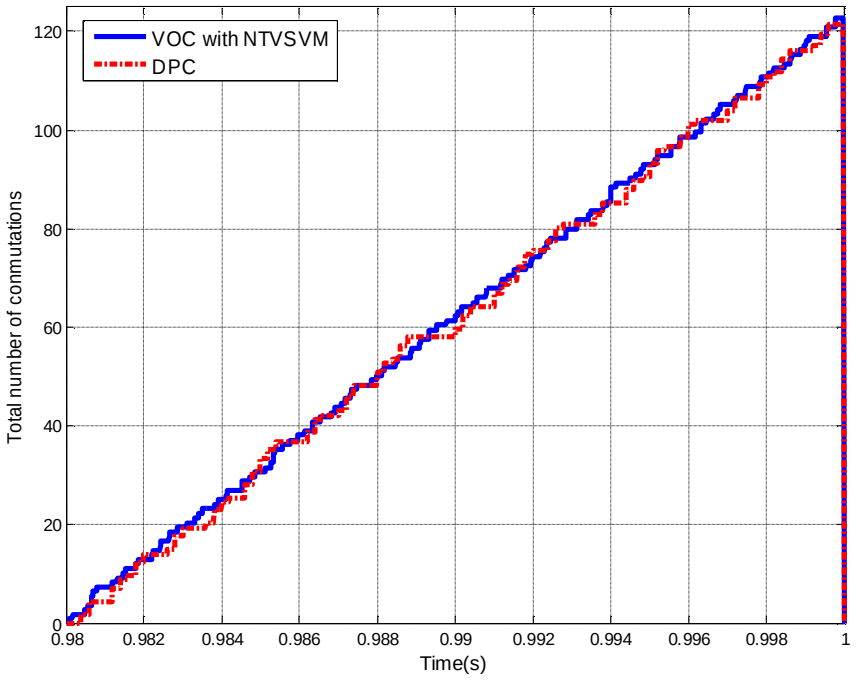


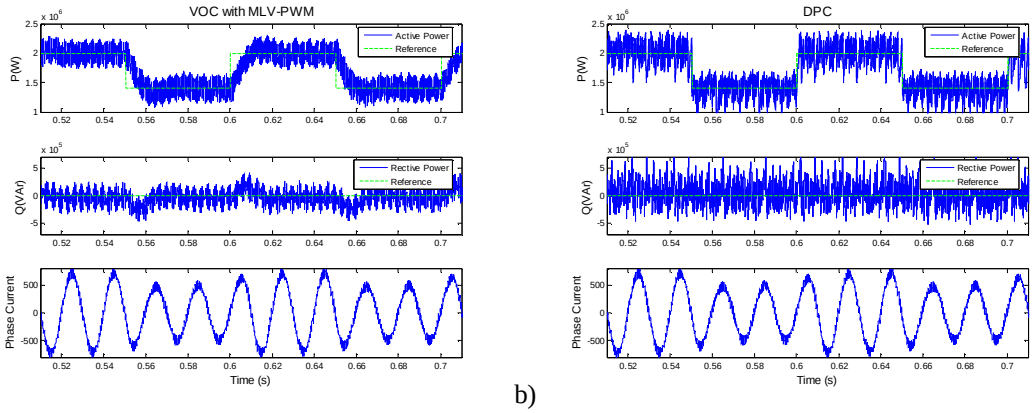
Fig.3.22: 3L-NPC VSI. Total number of commutations in a grid period

3.4.2. Transient Performance

Several simulations have been carried out in order to verify the behavior of the proposed control algorithms during transients. These simulations involve the 2L-VSI and 3L-NPC VSI configurations with the VOC and DPC-based control strategies. Active-power reference steps from 1.4MW to 2MW have been applied (30% of nominal power). Note that reactive power steps will produce similar results in transients, so these cases are not evaluated. Fig.3.23 shows the instantaneous active and reactive power behavior during active reference steps with the 2L-VSI configuration. As shown, the DPC is clearly faster than the VOC with MLV-PWM in power tracking task. The transient performance shows the expected behavior defined in section 3.2.2 in the VOC-based strategy, see Fig.3.24.

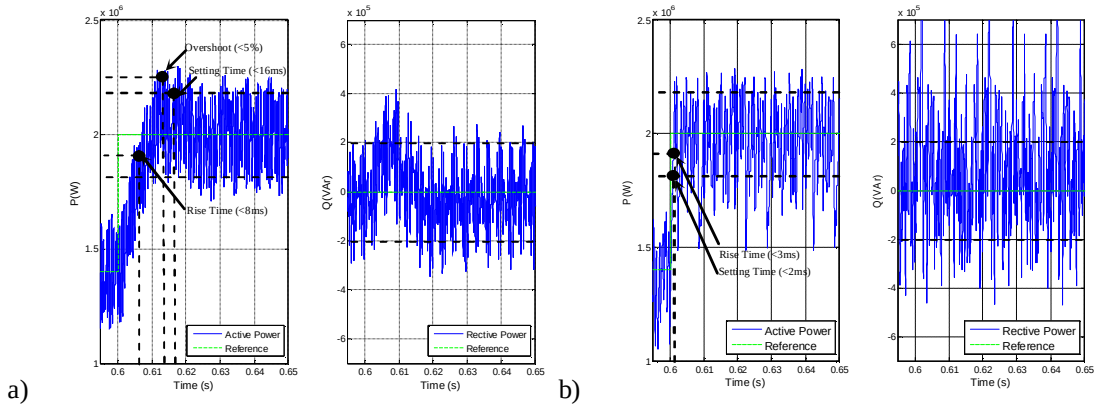
To quantify the transient behavior, a power band near 10% of the rated power is established. This way, a setting time close to 16ms, a rise time below 7ms and a small overshoot of around 5% can be observed in the VOC-based configuration. Yet, the DPC needs few ms (a setting time below 2ms with a rise time of around 3ms) without overshoot in power tracking requirements. Furthermore, there is no cross-coupling effect between active and reactive power in the DPC, whereas the VOC with MLV-PWM shows a substantial perturbation in the reactive power behavior when active power changes are applied.

In a similar way, several simulations considering the 3L-NPC VSI have been carried out. Fig.3.25 and Fig.3.26 show the instantaneous power behaviors under active power reference steps from 1.4MW to 2MW. These figures are coherent with the previous results related to the 2L-VSI in such a way that similar transients are obtained. Thus, the VOC with NTV-SVM shows a setting time, rise time and overshoot close to the design values, see Fig.3.26a. Also, it presents a cross-coupling effect between active and reactive power behaviors. On the other hand, the DPC shows a very fast transient response (it takes only 4ms instead of 15ms required by the VOC) without overshoot and cross-coupling effects.



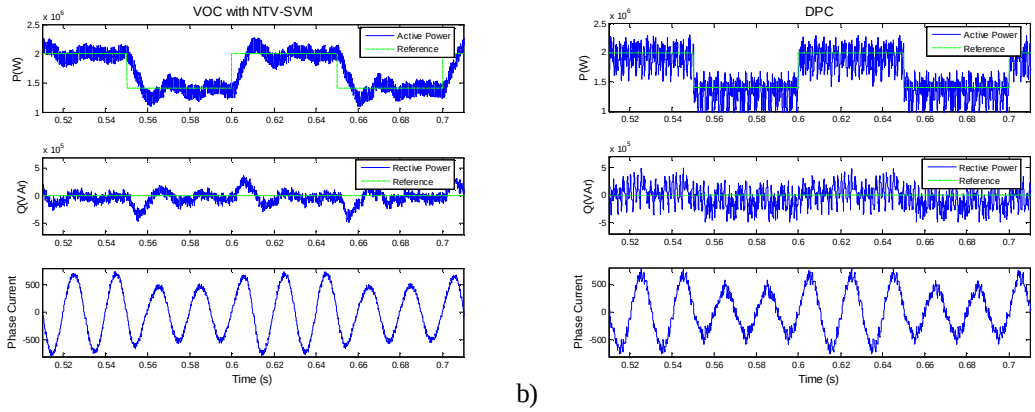
a) b)

Fig.3.23: 2L-VSI. Instantaneous active and reactive power behaviors during active reference steps: a) VOC with MLV-PWM b) DPC



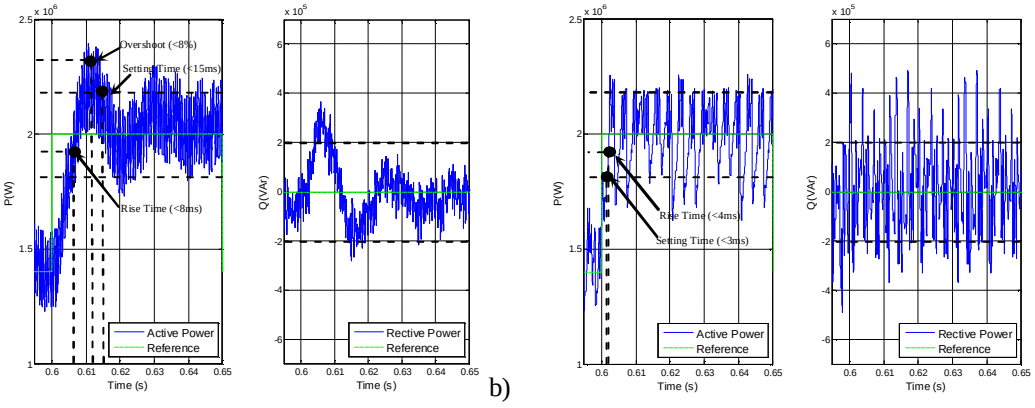
a) b)

Fig.3.24: 2L-VSI. Amplified active and reactive power transient behaviors: a) VOC with MLV-PWM b) DPC



a) b)

Fig.3.25: 3L-NPC VSI. Instantaneous active and reactive power behaviors during active reference steps: a) VOC with NTV-SVM b) DPC



a) b)

Fig.3.26: 3L-NPC VSI. Amplified active and reactive power transient behaviors: a) VOC with NTV-SVM b) DPC

3.5. Conclusions

The synthesis and analysis of two of the most interesting control methods for MV grid-connected operation conditions have been carried out. The first one is related to the widely employed VOC-type strategy and the second to the DPC which has become very popular in literature. Two different control strategies have been used in order to obtain good transient and steady-state performances.

With the aim to evaluate the proposed control algorithms, a coherent comparative frame toward each converter's topology has been defined. Hence, the same apparent switching frequency has been assumed, analyzing several steady-state and transient operation performances. The steady-state simulations show the best power quality features and the smaller power-tracking error in VOC-based strategies. On the other hand, DPC techniques offer the fastest transient behavior without overshoot and cross-coupling effect. Table 3.4 shows a brief description of the simulation results along with the characteristics and requirements of each control algorithm.

TABLE 3.4
CONTROL FEATURES AND REQUIREMENST

Features		**2L-VSI**		**3L-NPC VSI**	
		MLV-PWM	**DPC**	**NTV-SVM**	**DPC**
Switching Frequency		Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz	Constant f_{swMAX} = 6 kHz f_{Asw} =1kHz	Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz	Constant f_{swMAX} =5 kHz f_{Asw} =1kHz
Control & Sampling Period		$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$
Modulation Technique		MLV-PWM	-	NTV-SVM	-
Steady-state	**Current THD**	8%	15.85%	4.26%	10.78%
	Tracking Error	0.36%	9%	0.37%	6%
	Power Ripple	ΔP (12.37%) ΔQ (14.96%)	ΔP (20%) ΔQ (31.83%)	ΔP (9.15%) ΔQ (8.27%)	ΔP (18.58%) ΔQ (23.60%)
	DC-link Ripple	Δv_{DC} (0.14%) $Ic_{DC(RMS)}$(274.56A)	Δv_{DC} (0.34%) $Ic_{DC(RMS)}$(252.73A)	Δv_{DC} (0.11%) $Ic_{DC(RMS)}$(272.34)	Δv_{DC} (0.25%) $Ic_{DC(RMS)}$(250.15A)
Transient	**Cross-coupling Effect**	Yes	No	Yes	No
	Dynamic Performance	Setting time (<16ms) Rise time (<8ms) Overshoot (~5%)	Setting time (<2ms) Rise time (<3ms) Overshoot (-)	Setting time (<15ms) Rise time (<8ms) Overshoot (~8%)	Setting time (<3ms) Rise time (<4ms) Overshoot (-)

It is important to note that a basic DPC structure has been employed, so important improvements can be realized. In order to obtain both high transient dynamics and constant switching frequency, a new control approach based on DPC and predictive considerations is proposed in Chapter 4. This way, the developed approach will improve the steady-state performances while keeping the transient behavior.

Chapter 4

4. Predictive Direct Power Control

4.1. Introduction

This chapter describes the main contribution of this dissertation: the Predictive Direct Power Control (P-DPC), a new control approach where the well-known direct power control (DPC) is combined with a predictive selection of a voltage-vectors' sequence, obtaining both high transient dynamic and constant switching frequency. Four different P-DPC versions, which differ on the type of voltage-sequence used, are developed. Simulations of these strategies applied to grid-connected 2L and 3L-NPC VSIs under 2.3kV-2MWA operation conditions have been carried out. Thanks to its good transient behavior and its constant switching-frequency the P-DPC could become an interesting alternative of standard VOC techniques for grid-connected converters.

4.2. Predictive Direct Power Control. Theory and Application

The P-DPC selects the best voltage-vectors' sequences and computes their application times in order to control the power flow through the VSI under constant switching frequency operation. This strategy requires a predictive model of the instantaneous power behavior, which is explained next, followed by several possible control approaches.

4.2.1. Predictive Model of the Instantaneous Power Behavior in a line-connected VSI

P-DPC is based on the predictive model of the instantaneous active (P) and reactive (Q) power time-derivatives (4.1), which has been explained in Chapter 3 for a generic VSI with an L-type inductive filter.

$$\begin{aligned}\frac{dP}{dt} &= v_a\left(\frac{1}{L}\left(v_{Ka}-v_a\right)+w\,i_b\right)+v_b\left(\frac{1}{L}\left(v_{Kb}-v_b\right)-w\,i_a\right)\\ \frac{dQ}{dt} &= v_a\left(w\,i_a-\frac{1}{L}\left(v_{Kb}-v_b\right)\right)+v_b\left(\frac{1}{L}\left(v_{Ka}-v_a\right)+w\,i_b\right)\end{aligned} \tag{4.1}$$

The following considerations have been taken into account: any given voltage $v_k = [v_{k\alpha}\ v_{k\beta}]^T$ at the output of the VSI is kept constant during each voltage-vector application. In the same way, if the switching frequency is high enough, the line voltage $v = [v_\alpha\ v_\beta]^T$ can also be considered constant during the same period. Thus, and provided that current variations are small, quasi-constant active and reactive power evolutions can be considered during each voltage-vector application. These assumptions allow simple geometrical analysis of concatenated power evolutions. Active and reactive power-evolution slopes during a voltage-vector application are defined as follows:

$$\begin{aligned}f_{pi} &= \left.\frac{dP}{dt}\right|_{\vec{V}_k=\vec{V}_i}\\ f_{qi} &= \left.\frac{dQ}{dt}\right|_{\vec{V}_k=\vec{V}_i}\end{aligned} \tag{4.2}$$

Here *i* denotes the position index of the applied voltage in the sequence of voltage-vectors. Equation (4.3) computes the evolution of active and reactive powers under a given voltage-vector application during the related application time.

$$\begin{aligned} P_i &= P_{i-1} + f_{pi}\ t_{ai} \\ Q_i &= Q_{i-1} + f_{qi}\ t_{ai} \end{aligned} \tag{4.3}$$

And here $\{P_{i\text{-}1}\ Q_{i\text{-}1}\}$ indicates the initial active and reactive power values in the beginning of the *i*-th vector of the sequence, t_{ai} the application time and $\{P_i\ Q_i\}$ the active and reactive power values at the end of the application time.

4.2.2. P-DPC based on a Two Voltage-vectors' Sequence

The P-DPC strategy is based on the concatenation of several (4.3)-type trajectories along the control period, leading to the so-called voltage-vectors' sequence. This concatenation can be carried out in different ways, e.g., it can result in a non-symmetrical switching pattern containing two or three voltage vectors, or it can provide a symmetrical switching pattern combining two or three vectors, the so-called 2+2 or 3+3 voltage-vectors' sequence. This section will deal with the P-DPC based on the concatenation of two (4.3)-type trajectories along the control period T_{SW}. Fig. 4.1 shows an example containing a first steady state control period followed by an active power reference transient. In the beginning of each period the control must select two of the applicable voltage vectors and compute the required application times.

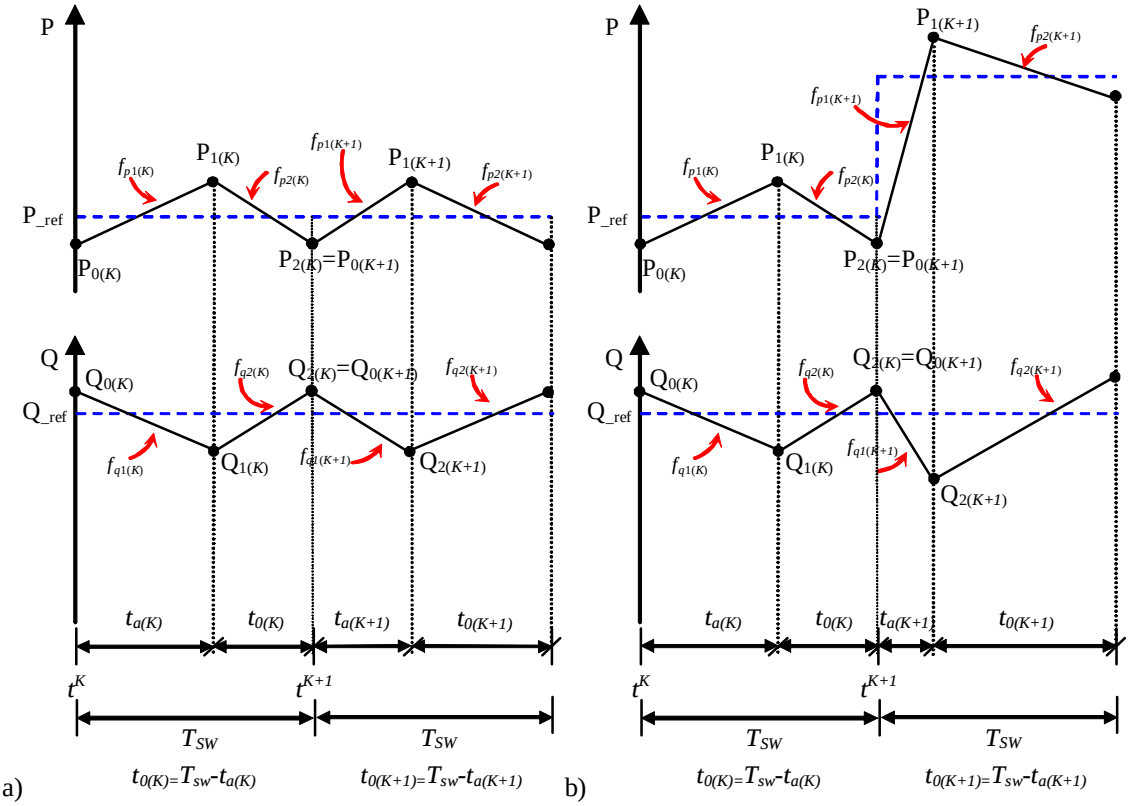


Fig. 4.1: Examples of the powers performance of P-DPC strategy based on two voltage vectors' sequence: a) Steady-state behavior b) Transient behavior during an active power reference step

4.2.2.1. Voltage-vectors' Selection

In this first approach the use of an active voltage-vector followed by a null vector is proposed. The active vector must be selected considering active and reactive-power time-derivatives defined in Chapter 3. On the other hand, the null vector is chosen in such a way that minimum switching actions occur in each control period. Hence, the selection of the best suited combination is carried out taking into account that active and reactive power tracking requirements will be fulfilled. This way, the following voltage-vectors' sequences have been proposed for the 2L and 3L-NPC VSIs, see Table 4.1 and Table 4.2. Note, that in the 3L-NPC VSI different voltage-vectors' sequences can be selected. As it has been pointed in previous sections, these extra degrees of freedom must be used in order to achieve complementary control requirements; as the DC-link voltage-balance.

TABLE 4.1
2L-VSI. VOLTAGE-VECTORS' SEQUENCES RELATED TO POWER REQUIREMENST

d*p*	**d*q***	θ_{1A}	θ_{1B}	θ_{2A}	θ_{2B}	θ_{3A}	θ_{3B}	θ_{4A}	θ_{4B}	θ_{5A}	θ_{5B}	θ_{6A}	θ_{6B}
1	**1**	v_{k6} / v_{k7}	v_{k1} / v_{k0}	v_{k1} / v_{k0}	v_{k2} / v_{k7}	v_{k2} / v_{k7}	v_{k3} / v_{k0}	v_{k3} / v_{k0}	v_{k4} / v_{k7}	v_{k4} / v_{k7}	v_{k5} / v_{k0}	v_{k5} / v_{k0}	v_{k6} / v_{k7}
1	**0**	v_{k1} / v_{k0}	v_{k2} / v_{k7}	v_{k2} / v_{k7}	v_{k3} / v_{k0}	v_{k3} / v_{k0}	v_{k4} / v_{k7}	v_{k4} / v_{k7}	v_{k5} / v_{k0}	v_{k5} / v_{k0}	v_{k6} / v_{k7}	v_{k6} / v_{k7}	v_{k1} / v_{k0}
0	**1**	v_{k0} / v_{k1}	v_{k7} / v_{k2}	v_{k7} / v_{k2}	v_{k0} / v_{k3}	v_{k0} / v_{k3}	v_{k7} / v_{k4}	v_{k7} / v_{k4}	v_{k0} / v_{k5}	v_{k0} / v_{k5}	v_{k7} / v_{k6}	v_{k7} / v_{k6}	v_{k0} / v_{k1}
0	**0**	v_{k7} / v_{k6}	v_{k0} / v_{k1}	v_{k0} / v_{k1}	v_{k7} / v_{k2}	v_{k7} / v_{k2}	v_{k0} / v_{k3}	v_{k0} / v_{k3}	v_{k7} / v_{k4}	v_{k7} / v_{k4}	v_{k0} / v_{k5}	v_{k0} / v_{k5}	v_{k7} / v_{k6}

TABLE 4.2
3L-NPC VSI. VOLTAGE-VECTORS' SEQUENCES RELATED TO POWER REQUIREMENST

d*p*	**d*q***	θ_{1A}	θ_{1B}	θ_{2A}	θ_{2B}	θ_{3A}	θ_{3B}
1	**1**	v_{k1_l} / v_{kz2}	v_{k1_l} / v_{kz2}	v_{k2_l} / v_{kz2}	v_{k2_l} / v_{kz2}	v_{k3_l} / v_{kz2}	v_{k3_l} / v_{kz2}
		v_{k6_m} / v_{kz0}	v_{k1_l} / v_{kz2}	v_{k1_m} / v_{kz0}	v_{k2_l} / v_{kz2}	v_{k2_m} / v_{kz0}	v_{k3_l} / v_{kz2}
1	**0**	v_{k1_m} / v_{kz0}	v_{k1_m} / v_{kz0}	v_{k2_m} / v_{kz0}	v_{k2_m} / v_{kz0}	v_{k3_m} / v_{kz0}	v_{k3_m} / v_{kz0}
0	**1**	v_{k1_s} / v_{kz1}	v_{k1_s} / v_{kz1}	v_{k2_s} / v_{kz1}	v_{k2_s} / v_{kz1}	v_{k3_s} / v_{kz1}	v_{k3_s} / v_{kz1}
0	**0**	v_{k1_s} / v_{kz1}	v_{k2_s} / v_{kz1}	v_{k2_s} / v_{kz1}	v_{k3_s} / v_{kz1}	v_{k3_s} / v_{kz1}	v_{k4_s} / v_{kz1}

d*p*	**d*q***	θ_{4A}	θ_{4B}	θ_{5A}	θ_{5B}	θ_{6A}	θ_{6B}
1	**1**	v_{k4_l} / v_{k21}	v_{k4_l} / v_{kz2}	v_{k5_l} / v_{kz2}	v_{k5_l} / v_{kz0}	v_{k6_l} / v_{kz2}	v_{k6_l} / v_{kz2}
		v_{k3_m} / v_{kz0}	v_{k4_l} / v_{kz2}	v_{k4_m} / v_{kz0}	v_{k5_l} / v_{kz2}	v_{k6_m} / v_{kz0}	v_{k6_l} / v_{kz2}
1	**0**	v_{k4_m} / v_{kz0}	v_{k4_m} / v_{kz0}	v_{k5_m} / v_{kz0}	v_{k5_m} / v_{kz0}	v_{k6_m} / v_{kz0}	v_{k6_m} / v_{kz0}
0	**1**	v_{k4_s} / v_{kz1}	v_{k4_s} / v_{kz1}	v_{k5_s} / v_{kz1}	v_{k5_s} / v_{kz1}	v_{k6_s} / v_{kz1}	v_{k6_s} / v_{kz1}
0	**0**	v_{k4_s} / v_{kz1}	v_{k5_s} / v_{kz1}	v_{k5_s} / v_{kz1}	v_{k6_s} / v_{kz1}	v_{k6_s} / v_{kz1}	v_{k1_s} / v_{kz1}

4.2.2.2. Application Times

Taking into account the equations (4.3) and the constant switching frequency condition, the set of equations defining the overall evolution of active and reactive powers during the control period (4.4) can be written, see Fig. 4.1.

$$\begin{aligned} P_1 &= P_0 + f_{p1}\, t_{a1} \quad / \quad Q_1 = Q_0 + f_{q1}\, t_{a1} \\ P_2 &= P_1 + f_{p2}\, t_0 \quad / \quad Q_2 = Q_1 + f_{q2}\, t_0 \\ T_{sw} &= t_{a1} + t_0 \end{aligned} \tag{4.4}$$

The control algorithm must compute the application time t_{a1} in such a way that controlled variables evolve from their initial values, $\{P_0\ Q_0\}$, towards the reference values, $\{P_2\ Q_2\}$. This problem has five equations and three variables, so an aproximative solution based on some optimization criteria must be computed. The algorithm must minimize the active and reactive power tracking errors, which are defined as:

$$\begin{aligned} e_{Fp} &= P_{\_ref} - P_0 - f_{p1}\, t_{a1} - f_{p2}\,(T_{SW} - t_{a1}) \\ e_{Fq} &= Q_{\_ref} - Q_0 - f_{q1}\, t_{a1} - f_{q2}\,(T_{SW} - t_{a1}) \end{aligned} \tag{4.5}$$

In order to use a least-square optimization method, next weight function is defined (4.6).

$$F = e_{Fp}^{\,2} + e_{Fq}^{\,2} \tag{4.6}$$

The optimal time of switching [t_{a1}] that minimizes the function $\boldsymbol{F}$ during a control period satisfies the minimum value condition:

$$\frac{\partial F}{\partial t_{a1}} = 0 \tag{4.7}$$

Solving the set of equations derived from (4.7) it is straightforward to get the next application times:

$$\begin{aligned} t_{a1} &= -\frac{\left[\begin{array}{l} -T_{SW}\cdot\left(f_{q2}^{\,2} + f_{p2}^{\,2}\right) + T_{SW}\cdot\left(f_{p2}\cdot f_{p1} + f_{q2}\cdot f_{q1}\right) \\ +e_{po}\cdot\left(f_{p2} - f_{p1}\right) + e_{qo}\cdot\left(f_{q2} - f_{q1}\right) \end{array}\right]}{\left(f_{p2} - f_{p1}\right)^2 + \left(f_{q2} - f_{q1}\right)^2} \\ t_0 &= T_{SW} - t_{a1} \end{aligned} \tag{4.8}$$

4.2.3. P-DPC based on a 2+2 Voltage-vectors' Sequence

This P-DPC version deals with the symmetrical 2+2 switching pattern example where the voltage-vectors' sequence is divided in two sub-sequences of two voltage-vectors each, see Fig.4.2. The second subsequence is symmetrical to the first one, i.e., it employs the same voltage-vectors and application times but reverses the application order. Thus, the last voltage vector of the first sequence matches up with the first voltage vector of the second sequence, leading to a switching frequency minimization. Fig.4.2 shows an example of power-trajectories concatenation under steady-state and transient operation. As in the previous P-DPC version, in the beginning of each control period the control must select the converter's voltage-vectors, followed by the computation of the required application times.

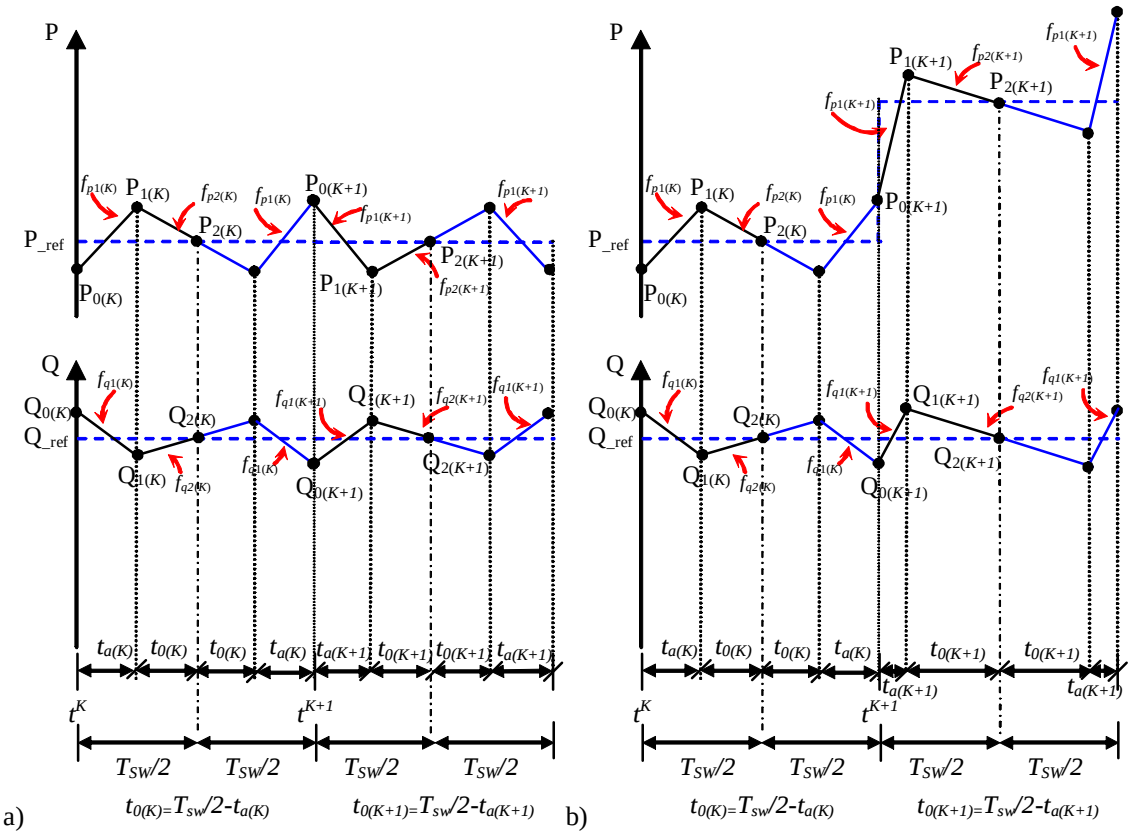


Fig.4.2: Examples of the powers performance of P-DPC strategy based on 2+2 voltage vectors' sequence: a) Steady-state behavior b) Transient behavior during an active power reference step

4.2.3.1. Voltage-vectors' Selection

In the same way as the P-DPC based on a two voltage-vectors' sequence does, the use of active and null voltage-vectors is proposed. Table 4.1 and Table 4.4 are considered for the 2L and 3L-NPC VSIs respectively. This way, a minimum number of commutations is generated in each control period leading to switching frequency minimization.

4.2.3.2. Application Times

In this case, the set of equations which define the overall behavior of active and reactive powers during the control period can be written as follows.

$$\begin{aligned} P_1 &= P_0 + 2 f_{p1}\, t_{a1} \quad / \quad Q_1 = Q_0 + 2 f_{q1}\, t_{a1} \\ P_2 &= P_1 + 2 f_{p2}\, t_0 \quad / \quad Q_2 = Q_1 + f_{q2}\, t_0 \\ \frac{T_{sw}}{2} &= t_{a1} + t_0 \end{aligned} \tag{4.9}$$

The control algorithm must compute the application time t_{a1} in such a way that controlled variables evolve from their initial values, $\{P_0\ Q_0\}$, towards the reference values, $\{P_2\ Q_2\}$. This problem has also

five equations and three variables. Consequently the same aproximative approach which has been developed in ***4.2.2.2*** is utilized. In this case the active and reactive-power tracking errors are defined as:

$$e_{Fp} = P_{\_ref} - P_0 - 2 f_{p1}\, t_{a1} - 2 f_{p2} \left(\frac{T_{SW}}{2} - t_{a1} \right)$$
$$e_{Fq} = Q_{\_ref} - Q_0 - 2 f_{q1}\, t_{a1} - 2 f_{q2} \left(\frac{T_{SW}}{2} - t_{a1} \right) \quad (4.10)$$

Solving the optimization problem stated by (4.6) and (4.7) the following application times are obtained.

$$t_{a1} = -\frac{\left[-\frac{T_{SW}}{2} \cdot \left(f_{q2}{}^2 + f_{p2}{}^2 \right) + \frac{T_{SW}}{2} \cdot \left(f_{p2} \cdot f_{p1} + f_{q2} \cdot f_{q1} \right) + e_{po} \cdot \left(f_{p2} - f_{p1} \right) + e_{qo} \cdot \left(f_{q2} - f_{q1} \right) \right]}{\left(f_{p2} - f_{p1} \right)^2 + \left(f_{q2} - f_{q1} \right)^2} \quad (4.11)$$
$$t_0 = \frac{T_{SW}}{2} - t_{a1}$$

4.2.4. P-DPC based on a Three Voltage-vectors' Sequence

The P-DPC using a three voltage-vectors' sequence is based on the optimal concatenation of three (4.3)-type trajectories along the control period T_{SW}. Fig.4.3 shows an example of this control version in a steady-state and transient operation. The P-DPC algorithm must select three of the applicable voltage vectors and the required application times in the beginning of each control period.

4.2.4.1. Voltage-vectors' Selection

The concatenation of three voltage-vectors offers an additional degree of freedom that can be used in order to reach complementary control objectives. This way, in the 2L-VSI case, the minimization of switching losses can be achieved following the main idea of MLV-PWM technique: the voltage vectors' sequence is chosen in such a way that the switching of a VSI leg does not happen during the maximum of line-current, leading to minimum switching losses (only two commutations per T_{SW} period). In the 3L-NPC VSI case, this extra degree of freedom makes it possible to minimize the number of commutations, to improve the power quality and to reduce the overall EMIs, in the same way that the NTV-SVM does.

The line-voltage plane is divided in a similar way as the DPC case of Chapter 3 does: six sectors of 60º, [θ_1.. θ_6] are divided in two subsectors, [θ_{iA}.. θ_{iB}], see Fig.3.7. Next, an example of vector selection will be discussed using Fig.4.4. This figure shows the first line-voltage quadrant composed by half of the sector 1 and the entire sector 2. The analysis carried out in this quadrant can be easily extended to any other quadrant. As the use of the nearest voltage-vectors provides the smallest current riple, when the grid voltage is located at any given sector, θ_i, the voltage application sequence must be built by neighboring voltage-vectors. This way, in the 2L-VSI case, the vectors' sequence is built by active voltage vectors

belonging to the set $\{\vec{v}_i, \vec{v}_{i-1}, \vec{v}_{i+1}\}$ and by one of the two null vectors, $\{\vec{v}_0, \vec{v}_7\}$, see Fig.4.4a. Conversely, in 3L-NPC VSI, the vectors' sequence must be built using voltage-vectors belonging to the set of large vectors $\{\vec{v}_{Ki\_l}, \vec{v}_{k(i-1)\_l}, \vec{v}_{k(i+1)\_l}\}$, medium vectors $\{\vec{v}_{Ki\_m}, \vec{v}_{k(i-1)\_m}, \vec{v}_{k(i+1)\_m}\}$, small vectors $\{\vec{v}_{Ki\_s}, \vec{v}_{k(i-1)\_s}, \vec{v}_{k(i+1)\_s}\}$ and null vectors, $\{\vec{v}_{z0}, \vec{v}_{z1}, \vec{v}_{z2}\}$, see Fig.4.4b. The apropriate sequence in both VSI-based configutarions will depend on the implied subsector and the switching-losses optimization strategy. In the first sector case, for example, the next two voltage application sequences are possible in the 2L-VSI.

$$q_1 \Rightarrow \{[\vec{v}_{k1}, \vec{v}_{k6}, \vec{v}_{k7}], [\vec{v}_{k1}, \vec{v}_{k2}, \vec{v}_{k7}]\} \tag{4.12}$$

In a similar way, expresion (4.13) shows the possible voltage vector's sequeces for 3L-NPC VSI.

$$q_1 \Rightarrow \left\{ \begin{matrix} [\vec{v}_{k1\_m}, \vec{v}_{k1\_l}, \vec{v}_{k1\_s}], [\vec{v}_{k2\_s}, \vec{v}_{k2\_l}, \vec{v}_{k1\_m}], \\ [\vec{v}_{k1\_m}, \vec{v}_{k2\_s}, \vec{v}_{k1\_s}], [\vec{v}_{kz1}, \vec{v}_{k2\_s}, \vec{v}_{k1\_s}] \end{matrix} \right\} \tag{4.13}$$

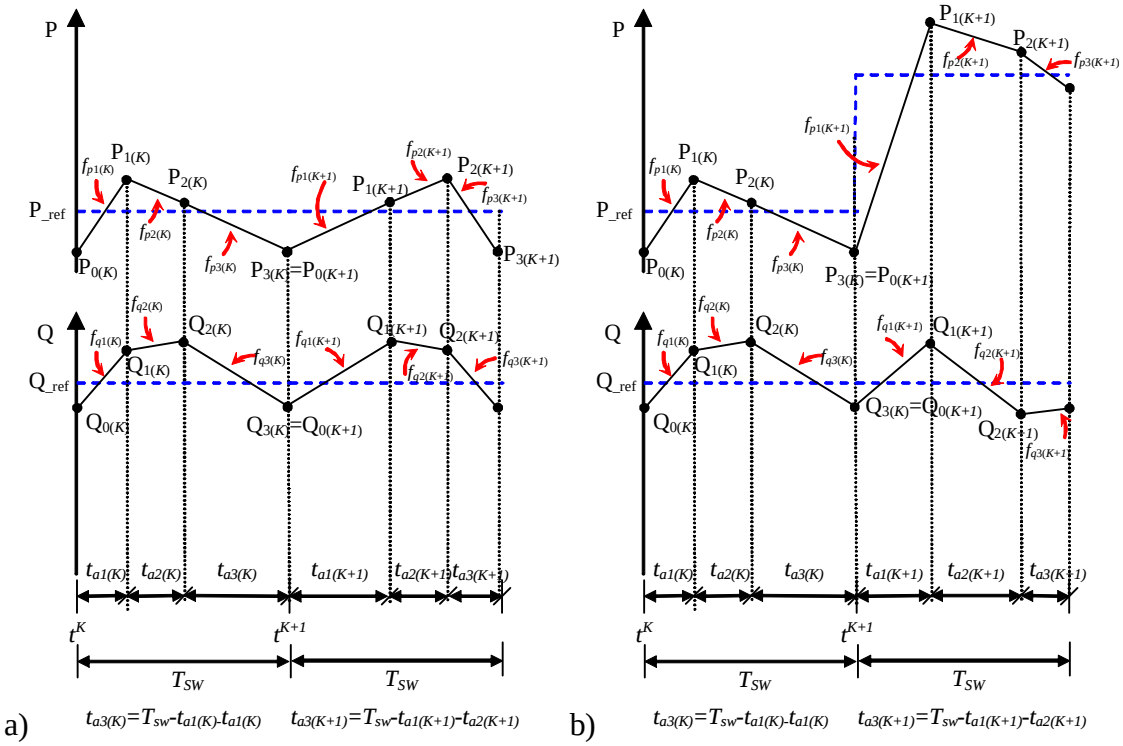


Fig.4.3: Examples of the powers performance of P-DPC strategy based on a three voltage vectors' sequence: a) Steady-state behavior b) Transient behavior during an active power reference step

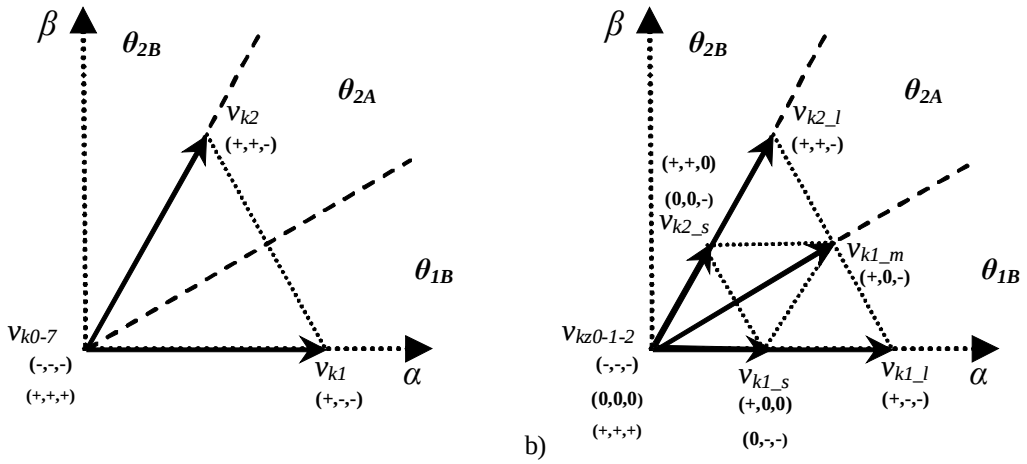


Fig.4.4: Set of available voltage-vectors on a three phase converter and mapping of the segments related to the line-voltage vector location: a) 2L-VSI, b) 3L-NPC VSI

DC-link Voltage Balance Requirements in 3L-NPC VSI

In the operation of 3L-NPC VSI it is important to keep the required voltage-balance in DC-link capacitors. Defining the converter's neutral-point-voltage unbalance as e_0, which can be denoted as neutral error, its time-evolution is given by equation (4.14).

$$\frac{de_0}{dt} = \frac{1}{C_{DC2}}\left[\left(S_{a2} - S_{a1}\right)i_a + \left(S_{b2} - S_{b1}\right)i_b + \left(S_{c2} - S_{c1}\right)i_c\right] \tag{4.14}$$

Here S_{xi} indicates the state of the switch number i belonging to the switching-leg x and i_x, the line current through the phase x, see Fig. 3.9. Making the same assumptions as in previous sections, a quasi-constant neutral-error evolution can be considered. Therefore it is possible to carry out a simple geometrical analysis of the concatenated neutral-error trajectories. Describing the slope of the linear evolution of the neutral-error during a voltage-vector application,

$$f_{e0i} = \left.\frac{de_0}{dt}\right|_{\vec{V}_k = \vec{V}_i} \tag{4.15}$$

the neutral-error at the end of the switching period is obtained:

$$e_{F0} = v_{DC1} - v_{DC2} - f_{e01}t_{a1} - f_{e02}t_{a2} - f_{e03}\left(T_{sw} - t_{a1} - t_{a2}\right) \tag{4.16}$$

The voltage vectors are selected in order to maintain the controlled *P-Q* variables close to the reference values. The fact is that some of these voltage vectors can be obtained by different switch configurations, implying different neutral-error evolutions. This redundancy, which is especially present in the "small voltage-vectors" family, provides an additional degree of freedom and is exploited in order to minimize the neutral-error value. The control algorithm must simply retain the redundant voltage-vector that minimizes the neutral-error (4.16).

4.2.4.2. Application Times

The set of equations defining the overall performance of active and reactive powers during the control period are:

$$\begin{aligned} P_1 &= P_0 + f_{p1}\, t_{a1} \quad / \quad Q_1 = Q_0 + f_{q1}\, t_{a1} \\ P_2 &= P_1 + f_{p2}\, t_{a2} \quad / \quad Q_2 = Q_1 + f_{q2}\, t_{a2} \\ P_3 &= P_2 + f_{p3}\, t_{a3} \quad / \quad Q_3 = Q_2 + f_{q3}\, t_{a3} \\ T_{sw} &= t_{a1} + t_{a2} + t_{a3} \end{aligned} \tag{4.17}$$

The control algorithm must compute the application times $\{t_{a1}, t_{a2}, t_{a3}\}$ in such a way that controlled variables evolve from their initial values, $\{P_0\ Q_0\}$, towards the reference values, $\{P_3\ Q_3\}$. The new problem has seven equations and six variables, therefore an aproximative solution based on a similar optimization criteria of the previous cases has been developed. The selected approach tries to minimize the active and reactive power tracking errors, which are defined as:

$$\begin{aligned} e_{Fp} &= P_{\_ref} - P_0 - f_{p1}t_{a1} - f_{p2}t_{a2} - f_{p3}(T_{sw} - t_{a1} - t_{a2}) \\ e_{Fq} &= Q_{\_ref} - Q_0 - f_{q1}t_{a1} - f_{q2}t_{a2} - f_{q3}(T_{sw} - t_{a1} - t_{a2}) \end{aligned} \tag{4.18}$$

In the same way, a least-square optimization method is used, trying to minimize the weight function of equation (4.19).

$$F = {e_{Fp}}^2 + {e_{Fq}}^2 \tag{4.19}$$

The optimal set of application times that minimizes the function ***F*** during a control period satisfies the next two minimum value conditions:

$$\begin{cases} \dfrac{\partial \mathrm{F}}{\partial \mathrm{t}_{a1}} = 0 \\ \dfrac{\partial \mathrm{F}}{\partial \mathrm{t}_{a2}} = 0 \end{cases} \tag{4.20}$$

Replacing (4.18) in (4.19) we get the weight function of the form:

$$F = f(t_{a1}, t_{a2}) \tag{4.21}$$

The sensitivity of this function against t_{a1} and t_{a2} is shown in equation (4.22).

$$\begin{cases} \dfrac{dF}{dt_{a1}} = 2\left(e_{p0} - 2f_{p1}t_{a1} - 2f_{p2}t_{a2} - 2f_{p3}\left(\dfrac{1}{2}T_{sw} - t_{a1} - t_{a2}\right)\right)\left(-2f_{p1} + 2f_{p3}\right) \\ \quad + 2\left(e_{q0} - 2f_{q1}t_{a1} - 2f_{q2}t_{a2} - 2f_{q3}\left(\dfrac{1}{2}T_{sw} - t_{a1} - t_{a2}\right)\right)\left(-2f_{q1} + 2f_{q3}\right) = 0 \\ \dfrac{dF}{dt_{a2}} = 2\left(e_{p0} - 2f_{p1}t_{a1} - 2f_{p2}t_{a2} - 2f_{p3}\left(\dfrac{1}{2}T_{sw} - t_{a1} - t_{a2}\right)\right)\left(-2f_{p2} + 2f_{p3}\right) \\ \quad + 2\left(e_{q0} - 2f_{q1}t_{a1} - 2f_{q2}t_{a2} - 2f_{q3}\left(\dfrac{1}{2}T_{sw} - t_{a1} - t_{a2}\right)\right)\left(-2f_{q2} + 2f_{q3}\right) = 0 \end{cases} \tag{4.22}$$

The minimum of $\boldsymbol{F}$ is reached when the values of the two sensitivity functions are equal to zero. The resulting set of two equations and two variables can be easily computed, leading to the solution shown in (4.23).

$$
\begin{aligned}
t_{a1} &= \frac{\left[\begin{array}{l}\left(f_{q2}-f_{q3}\right)\cdot e_{po}+\left(f_{p3}-f_{p2}\right)\cdot e_{qo}\\ +\left(f_{q3}\cdot f_{p2}-f_{q2}\cdot f_{p3}\right)\cdot T_{SW}\end{array}\right]}{\left[\begin{array}{l}f_{q3}\cdot f_{p2}-f_{q1}\cdot f_{p2}-f_{q2}\cdot f_{p3}\\ +f_{q1}\cdot f_{p3}-f_{q3}\cdot f_{p1}+f_{q2}\cdot f_{p1}\end{array}\right]} \\
t_{a2} &= \frac{\left[\begin{array}{l}\left(f_{q3}-f_{q1}\right)\cdot e_{po}+\left(f_{p1}-f_{p3}\right)\cdot e_{qo}\\ +\left(-f_{q3}\cdot f_{p1}+f_{q1}\cdot f_{p3}\right)\cdot T_{SW}\end{array}\right]}{\left[\begin{array}{l}f_{q3}\cdot f_{p2}-f_{q1}\cdot f_{p2}-f_{q2}\cdot f_{p3}\\ +f_{q1}\cdot f_{p3}-f_{q3}\cdot f_{p1}+f_{q2}\cdot f_{p1}\end{array}\right]} \\
t_{a3} &= T_{SW}-t_{a1}-t_{a2}
\end{aligned}
\tag{4.23}
$$

4.2.5. P-DPC based on a 3+3 Voltage-vectors' Sequence

This control approach employs the symmetrical 3+3 switching pattern, in such a way that the voltage-vectors' sequence is divided in two sub-sequences of three voltage-vectors each, see Fig.4.5. This control strategy is an extended version of the P-DPC based on a 2+2 voltage-vector' sequence. As shown, the second subsequence is symmetrical to the first one (it employs the same voltage-vectors and application times but reverses the application order), allowing the switching-frequency minimization. As previous versions, the control must select three of the applicable voltage vectors followed by the application times in the beginning of each control period. Fig.4.5 shows an example of power trajectories under steady-state and transient operations.

4.2.5.1. Voltage-vectors' Selection

The selection of voltage vectors has been developed taking into account the same considerations assumed for P-DPC based on a three voltage-vectors' sequence version. This way, the line-voltage plane is divided in six sectors of 60º, [θ_1.. θ_6], which are also divided in two subsectors, [θ_{iA}.. θ_{iB}], see Fig.3.7. The use of the nearest voltage-vectors is considered, so when the grid voltage is located at any given sector, θ_i, each voltage application subsequence is built by the neighboring voltage-vectors. In the first sector case, for example, voltage vectors belonging to the sets (4.12) and (4.13) can be employed as part of first sub-sequence and the last sub-sequence must be symmetrical to the first one.

DC-link Voltage Balance Requirements in 3L-NPC VSI

The DC-link voltage-balance is required in 3L-NPC VSI steady-state operation. As proposed in ***4.2.4.1*** it is possible to carry out a simple geometrical analysis of the concatenated neutral-error trajectories where the neutral-error at the end of the switching period is described as:

$$e_{F0} = v_{DC1} - v_{DC2} - 2 f_{e01} t_{a1} - 2 f_{e02} t_{a2} - 2 f_{e03} \left(\frac{T_{sw}}{2} - t_{a1} - t_{a2} \right) \tag{4.24}$$

Thus, the voltage vectors are selected in order to keep the controlled *P-Q* variables close to the reference values fulfilling the DC-link voltage-balance requirements.

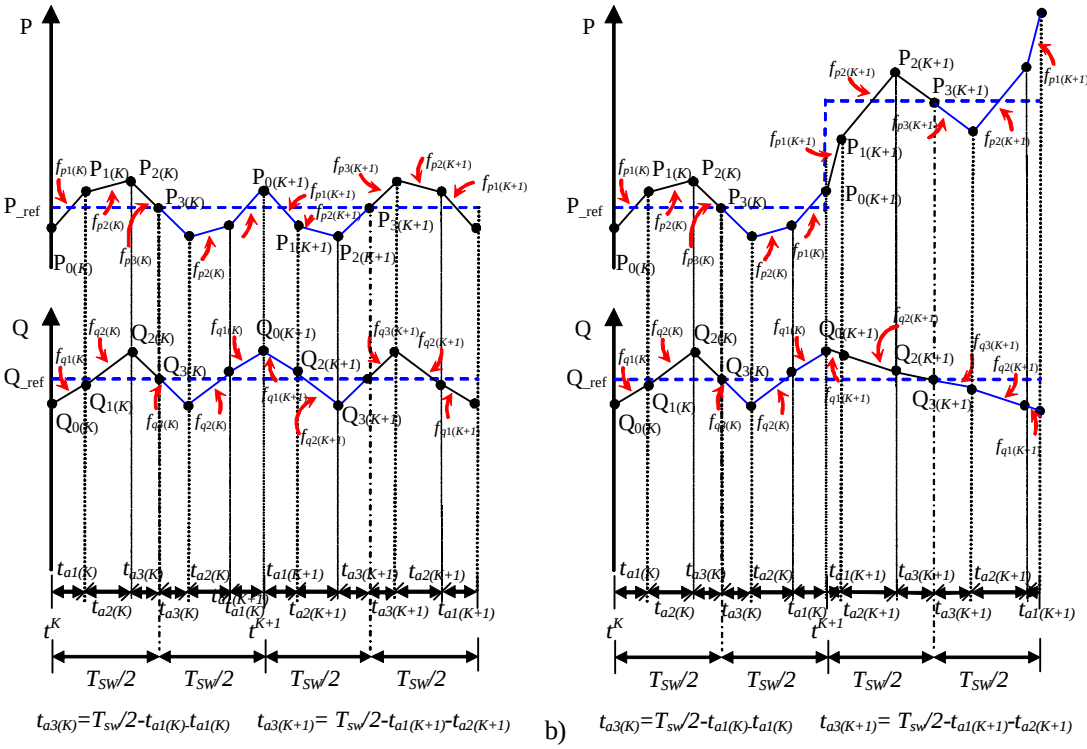


Fig.4.5: Examples of the powers' performance of P-DPC strategy based on a 3+3 voltage vectors' sequence: a) Steady-state behavior b) Transient behavior during an active power reference step

4.2.5.2. Application Times

Combining equations (4.3) with the constant switching frequency constraint, it is possible to get the set of equations which define the active and reactive-power behavior during the voltage-vectors' sequence:

$$\begin{aligned} P_1 &= P_0 + 2 f_{p1}\, t_{a1} \quad / \quad Q_1 = Q_0 + 2 f_{q1}\, t_{a1} \\ P_2 &= P_1 + 2 f_{p2}\, t_{a2} \quad / \quad Q_2 = Q_1 + 2 f_{q2}\, t_{a2} \\ P_3 &= P_2 + 2 f_{p3}\, t_{a3} \quad / \quad Q_3 = Q_2 + 2 f_{q3}\, t_{a3} \\ \frac{T_{sw}}{2} &= t_{a1} + t_{a2} + t_{a3} \end{aligned} \tag{4.25}$$

As in the previous P-DPC version, the control algorithm must compute the application times $\{t_{a1}, t_{a2}, t_{a3}\}$ in such a way that controlled variables evolve from their initial values, $\{P_0\ Q_0\}$, towards the reference values, $\{P_3\ Q_3\}$. Similarly, the problem has seven equations and six variables, therefore an approximate solution based on the optimization criteria employed in ***4.2.4.2*** is used. The new active and reactive-power tracking errors are defined as follows.

$$\begin{aligned} e_{Fp} &= P_{\_ref} - P_0 - 2f_{p1}t_{a1} - 2f_{p2}t_{a2} - 2f_{p3}\left(\frac{T_{sw}}{2} - t_{a1} - t_{a2}\right) \\ e_{Fq} &= Q_{\_ref} - Q_0 - 2f_{q1}t_{a1} - 2f_{q2}t_{a2} - 2f_{q3}\left(\frac{T_{sw}}{2} - t_{a1} - t_{a2}\right) \end{aligned} \tag{4.26}$$

Considering (4.19) and (4.20) it is straightforward to get the next application times:

$$\begin{aligned} t_{a1} &= \frac{\left[\begin{array}{l}\left(f_{q2} - f_{q3}\right)\cdot e_{po} + \left(f_{p3} - f_{p2}\right)\cdot e_{qo} \\ + \left(f_{q3}\cdot f_{p2} - f_{q2}\cdot f_{p3}\right)\cdot \dfrac{T_{SW}}{2}\end{array}\right]}{\left[\begin{array}{l} f_{q3}\cdot f_{p2} - f_{q1}\cdot f_{p2} - f_{q2}\cdot f_{p3} \\ + f_{q1}\cdot f_{p3} - f_{q3}\cdot f_{p1} + f_{q2}\cdot f_{p1}\end{array}\right]} \\ t_{a2} &= \frac{\left[\begin{array}{l}\left(f_{q3} - f_{q1}\right)\cdot e_{po} + \left(f_{p1} - f_{p3}\right)\cdot e_{qo} \\ + \left(-f_{q3}\cdot f_{p1} + f_{q1}\cdot f_{p3}\right)\cdot \dfrac{T_{SW}}{2}\end{array}\right]}{\left[\begin{array}{l} f_{q3}\cdot f_{p2} - f_{q1}\cdot f_{p2} - f_{q2}\cdot f_{p3} \\ + f_{q1}\cdot f_{p3} - f_{q3}\cdot f_{p1} + f_{q2}\cdot f_{p1}\end{array}\right]} \\ t_{a3} &= \frac{T_{SW}}{2} - t_{a1} - t_{a2} \end{aligned} \tag{4.27}$$

4.3. Control System Configuration

The block diagrams of the proposed P-DPC approaches are shown in Fig.4.6. Initial line-voltage and current values are required in order to compute initial active and reactive powers [P_0, Q_0]. The control algorithm evaluates this information and the reference-power values, selects the appropriate sequence and computes the application times which minimize the final tracking errors. In addition, the 3L-NPC VSI configuration considers the DC-link voltage dynamics in order to keep the required voltage-balanced in the DC-link capacitors, see Fig.4.7.

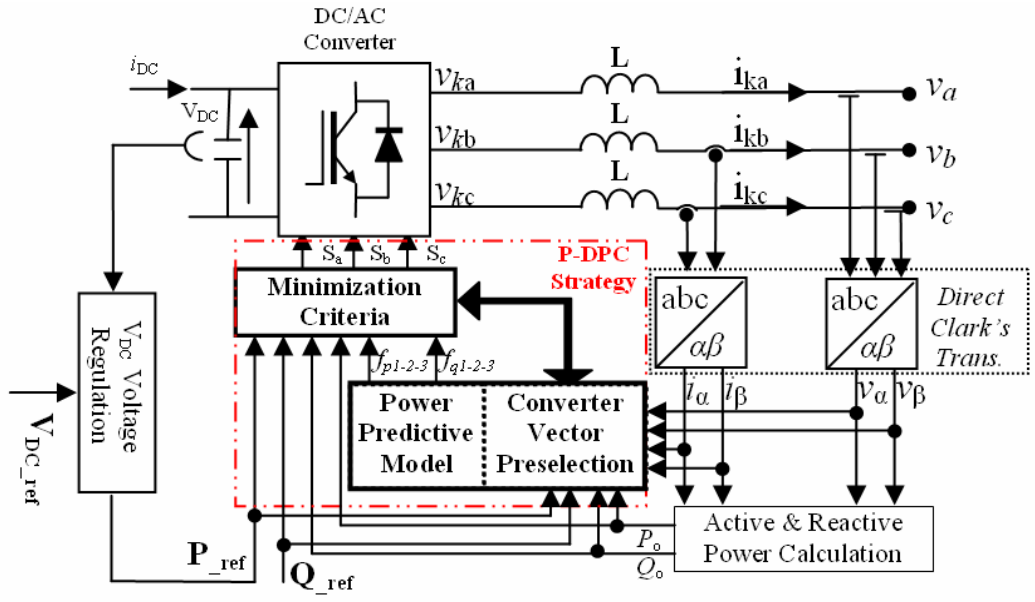


Fig.4.6: P-DPC system's block diagrams of 2L-VSI

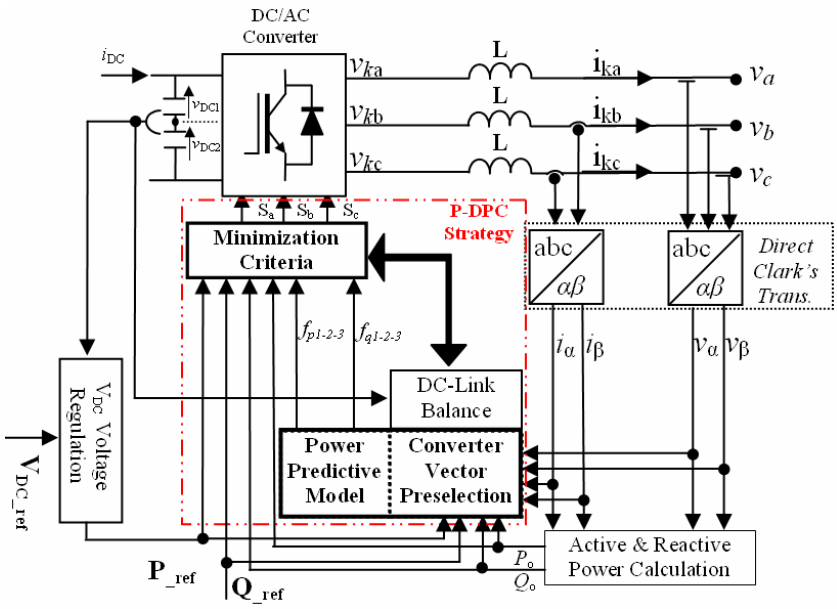


Fig.4.7: P-DPC system's block diagrams of 3L-NPC VSI

Fig.4.8 and Fig.4.9 show four flowcharts summarizing the main P-DPC strategies. All of them can can exploit any of the previously explained voltage vectors' sequences: the simple 2 or 3 vectors' sequence or the symmetrical 2+2 or 3+3 voltage sequences.

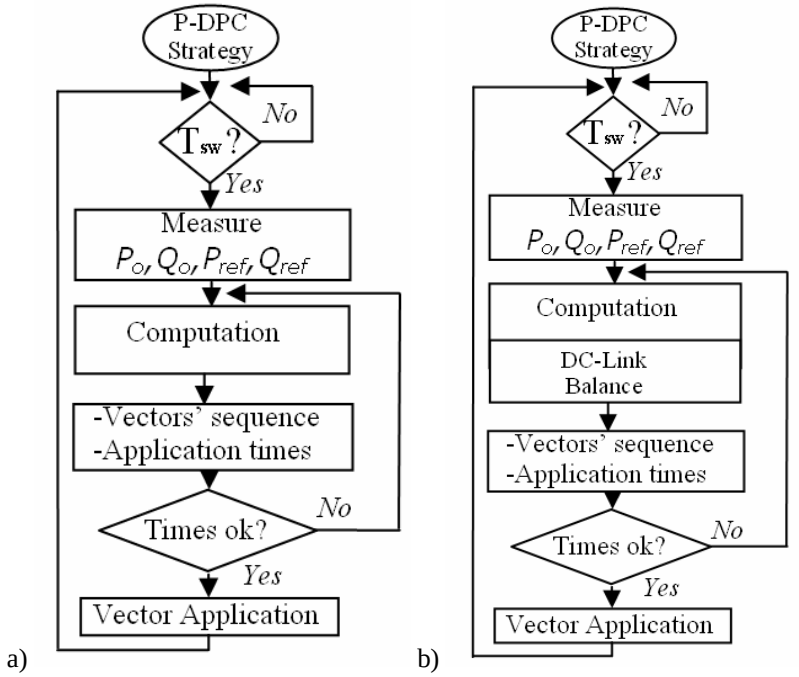


Fig.4.8: Simple P-DPC-based flowcharts: a) 2L-VSI, b) 3L-NPC VSI

In the beginning of each control period the active and reactive-powers are computed using instantaneous current and voltage measures. Then, the P-DPC algorithm selects the optimum voltage vectors' sequence and the related application times (using any of the P-DPC versions), taking into account the power tracking requirements. The selected voltage-vectors are applied during the computed application times, completing the control period.

Hybrid P-DPC strategies could be also proposed, see Fig.4.9. The main idea here is to make use of a large set of concatenated-voltage vectors only in steady state operation, improving efficiency and current ripple. The advantages of a simple set of two concatenated-voltage vectors are exploited in transients. The steady-state strategy employs the nearest active voltage-vectors improving the steady-state performance. Obviously this is not the best strategy for transients, where other far active voltage-vectors would provide faster responses. Because of this, for transients, the voltage sequence must be built by the voltage vector which generates the fastest evolution on the desired direction, i.e., the best-oriented larger active vector, followed by a null vector. In the 2L-VSI, all active vectors are evaluated whereas in the 3L-NPC VSI case only large vectors are considered. The proposed hybrid configuration will need few μs to identify whether a transient is required or not, select the best voltage-vectors' sequence and compute the application times. Finally, the voltage-vectors will be applied during the computed application times within the control period.

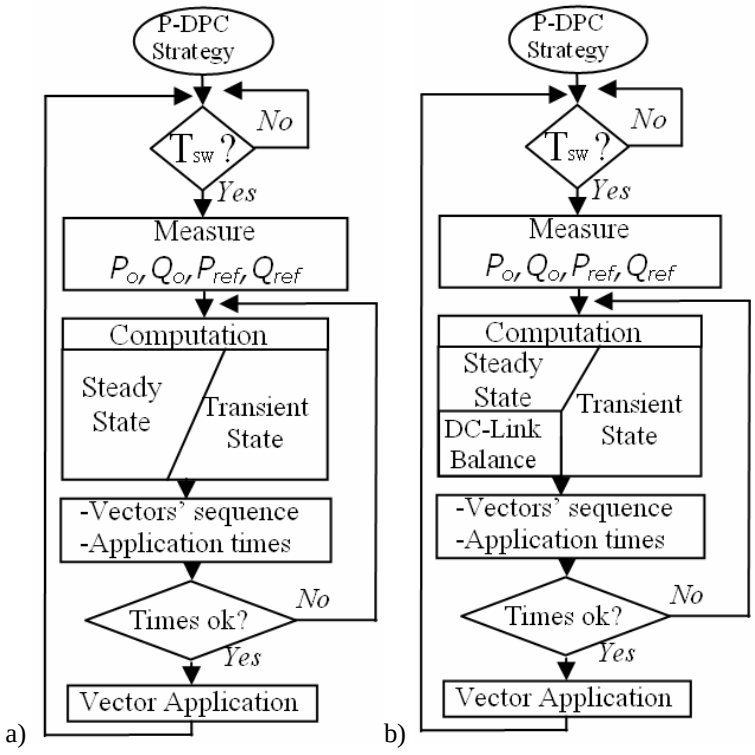


Fig.4.9: Hybrid P-DPC-based flowcharts: a) 2L-VSI, b) 3L-NPC VSI

4.4. Simulation Results

In order to verify the behavior of the proposed control algorithms, several simulations involving the basic versions of P-DPC have been carried out. All control strategies are evaluated under steady and transient operation conditions and results of the non-symmetrical switching patterns are compared to the behavior of the symmetrical versions. The specifications and parameters are listed in Table 2.3 from Chapter 2. Besides, the main control features and requirements of proposed control strategies both in the 2L and 3L-NPC VSIs are summarized in Table 4.1. All the proposed P-DPC strategies are designed in order to operate at the same apparent switching frequency.

TABLE 4.1
MAIN CHARACTERISTICS OF P-DPC-BASED CONTROL STRATEGIES

	Version	Apparent Switching Frequency	Control & Sampling Frequency
P-DPC	Two voltage-vectors' sequence	1 [kHz]	3 [kHz]
	2+2 voltage-vectors' sequence	1 [kHz]	3 [kHz]
	Three voltage-vectors' sequence	1 [kHz]	1.5 [kHz]
	3+3 voltage-vectors' sequence	1 [kHz]	1.5 [kHz]

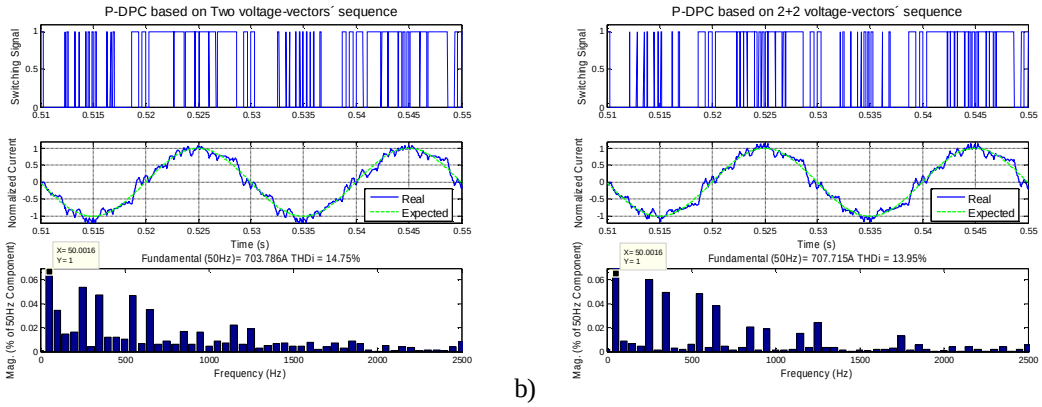
4.4.1. Steady-state Performance

First simulation have been carried out considering the 2L-VSI under P-DPC using whether a simple 2 voltage-vectors sequence or a symmetrical 2+2 one. Fig.4.10 summarizes the resulting per-phase switching pattern, normalized line current and frequency spectrum. The line current waveforms are strongly distorted and the THD measurements are close to 14% in both cases. Therefore, the IEEE Std.

519-1992 recommendation is not fulfilled. In addition, low-frequency odd harmonics are generated in any case. In spite of this, the absolute tracking errors are substantially small. If the non-symmetrical switching pattern is used, it is close to 0.87% and it is around 0.32% when the symmetrical version is considered.

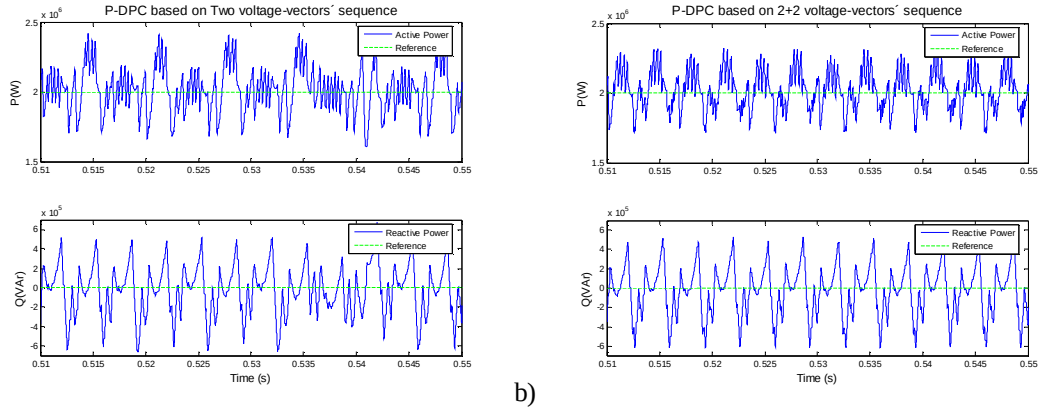
The ripples of both the active-power and the DC-link voltage are slightly smaller when a symmetrical voltage-vectors' sequence is used, see Fig.4.11 and Fig.4.12. In fact, non-symmetrical switching pattern-based strategy shows active and reactive-power ripples of around 22% and 33%, whereas they fall down to 18% and 34% when a symmetrical switching pattern is applied. When the two voltage-vectors' based P-DPC version is used the DC-link voltage ripple is around 0.23% with an RMS current across the DC capacitor of 277A. If the symmetrical 3+3 sequence is used, the DC-link voltage ripple fall down to 0.16% and the RMS current is maintained at 277A.

Finally, detailed behaviors of several variables are shown in Fig.4.13. As can be observed, quasi-linear active and reactive power trajectories evolve around the reference values along three control periods.



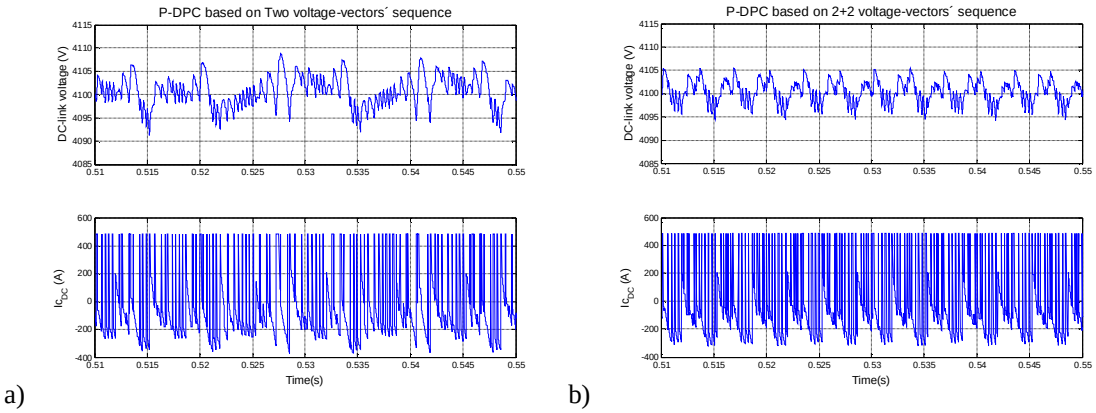
a) b)

Fig.4.10: 2L-VSI. Phase switching signals, normalized line current and frequency spectrum: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence



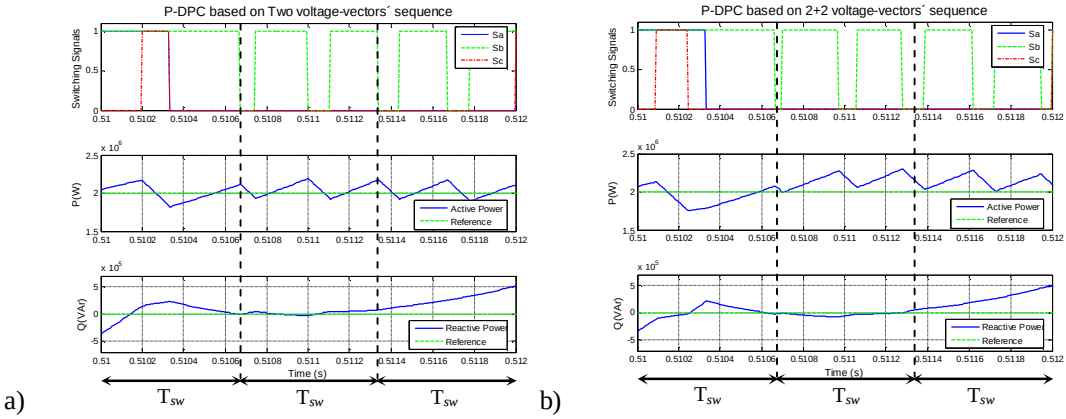
a) b)

Fig.4.11: 2L-VSI. Active and reactive power behaviors: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence



a) b)

Fig.4.12: 2L- VSI. DC-link voltage and capacitor's current ripple: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence



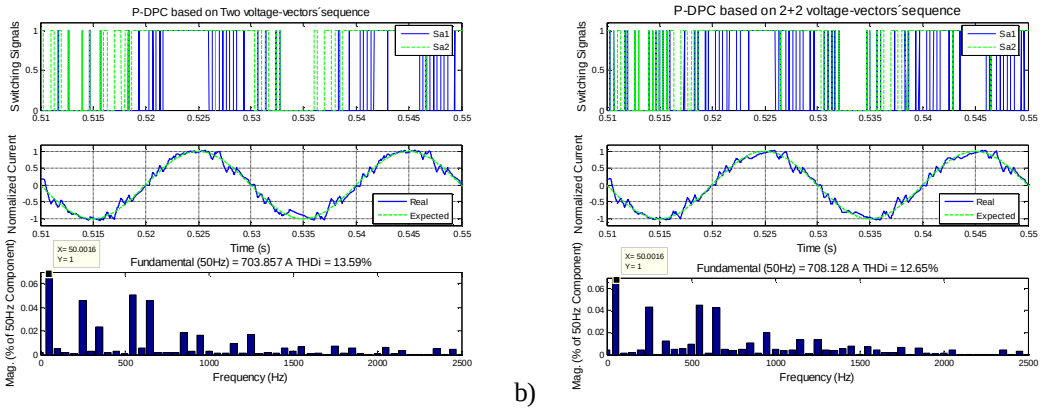
a) b)

Fig.4.13: 2L- VSI. Switching signals and active and reactive power trajectories along three control periods: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence

In a similar way, Fig.4.14 shows the per-phase switching signals, normalized line current and frequency spectrum of the 3L-NPC VSI with a P-DPC based on a simple 2 and symmetrical 2+2 voltage-vectors' sequences. Compared to the 2L-VSI there are not significant improvements. The low odd harmonics have been reduced, decreasing the current THD to almost 13% in both cases. As a result, the IEEE Std. 519-1992 is not fulfilled, leading to the conclusion that these P-DPC versions are not appropriate to generate a good current quality under the required specifications. The absolute tracking errors are 0.73% for the single sequence version and 0.33% for the symmetrical case.

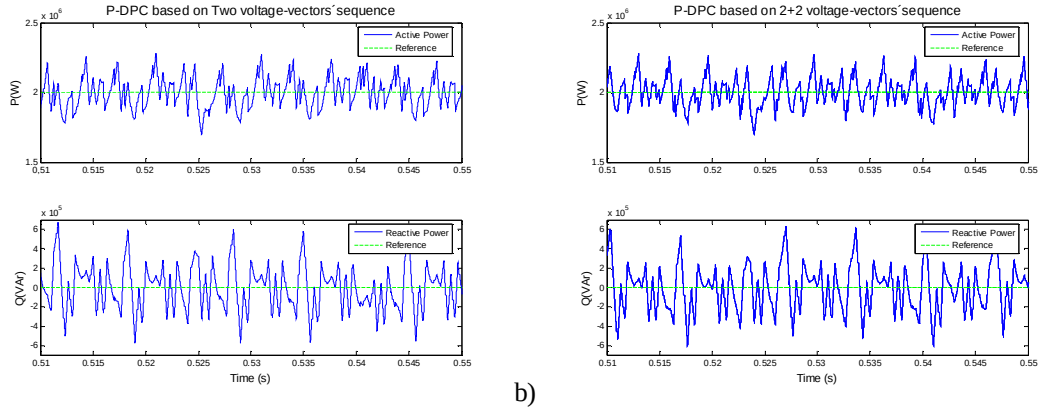
The power and DC-link-voltage ripples are also slightly improved under the symmetrical switching pattern against the non-symmetrical P-DPC version, see Fig.4.15 and Fig.4.16. In the first case, the active and reactive-power ripple values are around 22% and 36% respectively. In the case of the symmetrical 2+2 version, these values fall down to 15% and 33%. Analyzing the DC-link behavior, the non-symmetrical P-DPC strategy establishes a voltage ripple of 0.23% with an RMS current across the capacitors of around 240A. On the other hand, the symmetrical version provides a lower voltage ripple of 0.17% and the same RMS current of 239A. It is important to note that both control approaches show a perturbation in the voltage of DC-link capacitors located at the typical frequency of 150Hz which is characteristic of three-level converters with some kind of SVM. The behavior of these P-DPC versions

along three control periods is shown in Fig.4.17. In a similar way to previous strategies, quasi-linear trajectories evolve around the reference values.



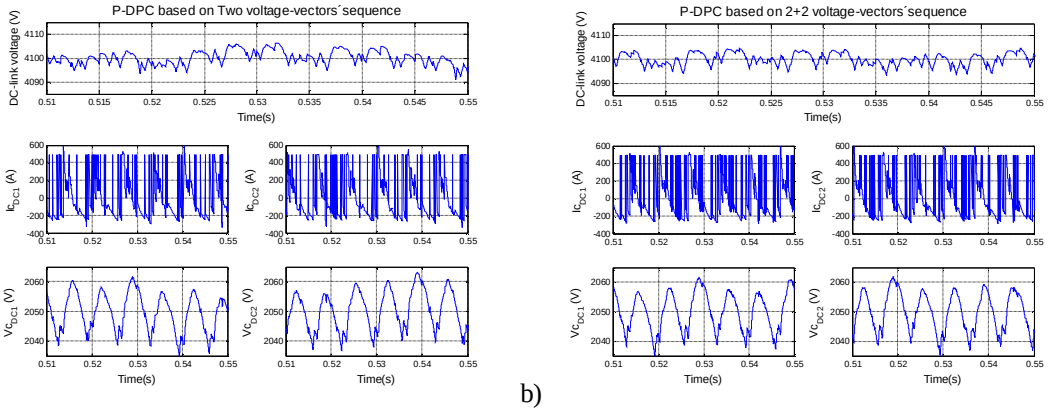
a) b)

Fig.4.14: 3L-NPC VSI. Phase switching signals, normalized line current and frequency spectrum: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence



a) b)

Fig.4.15: 3L-NPC VSI. Active and reactive power behaviors: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence



a) b)

Fig.4.16: 3L-NPC VSI. DC-link voltage and capacitor's current ripple: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence

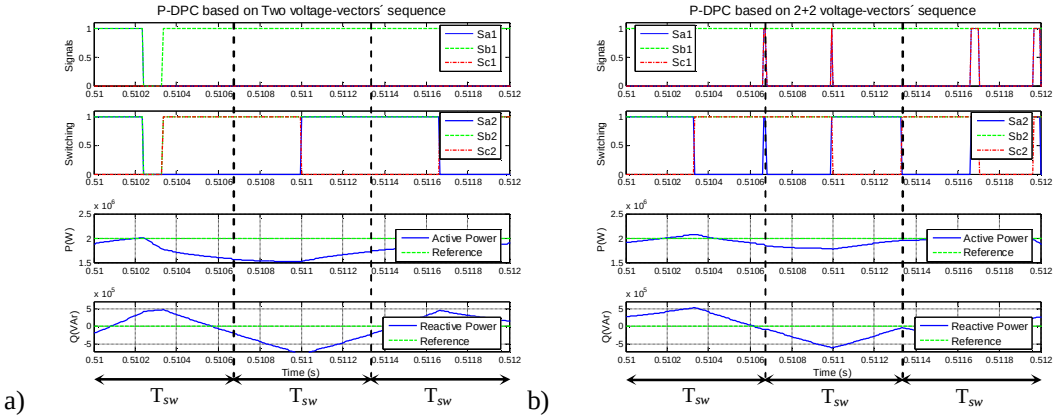


Fig.4.17: 3L-NPC VSI. Switching signals and active and reactive power trajectories along three control periods: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence

Fig.4.18 shows the per-phase switching signals, line current and frequency spectrum related to the 2L-VSI with P-DPC strategies using both a simple three voltage-vectors' sequence and a symmetrical 3+3 one. It can be observed that there are no switching actions along the maximum of the line current in these versions, thus improving the converter's power-losses. When the simple sequence is used, a considerable current ripple is observed, which implies a high harmonic content (THD_i=14%). On the other hand, if the symmetrical version is used the harmonic spectrum and THD are substantially reduced (THDi=7.6%), see Fig.4.18b. In this case, better current quality than previous versions can be obtained, but the IEEE Std. 519-1992 recommendation is not yet fulfilled. The absolute tracking errors are around 0.86% and 0.46% in the non-symmetrical and symmetrical P-DPC versions respectively. The improvement using the symmetrical-based P-DPC version can be clearly observed in the power and DC-link voltage-ripple performance, see Fig.4.19 and Fig.4.20. Hence, the non-symmetrical switching pattern-based P-DPC version shows active and reactive power ripple values close to 25% and 21%. The symmetrical version becomes the most interesting alternative (ΔP=14%, ΔQ=12%). In a similar way, from the point of view of the DC-link, the symmetrical version shows the best solution (Δv_{DC}=0.12%,$Ic_{DC(RMS)}$=275A) against the non-symmetrical technique (Δv_{DC}=0.28%, $Ic_{DC(RMS)}$=281A). The switching pattern of both control strategies can be easily derived from active and reactive power trajectories which are shown in Fig.4.21.

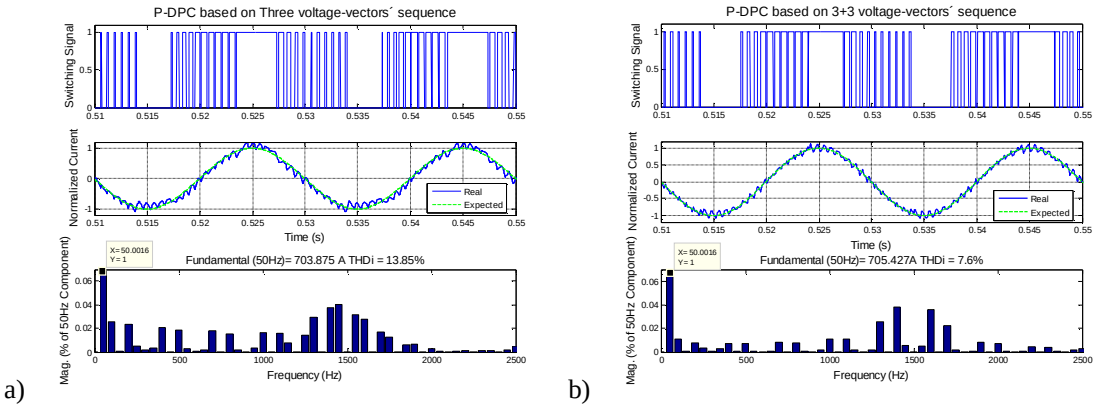
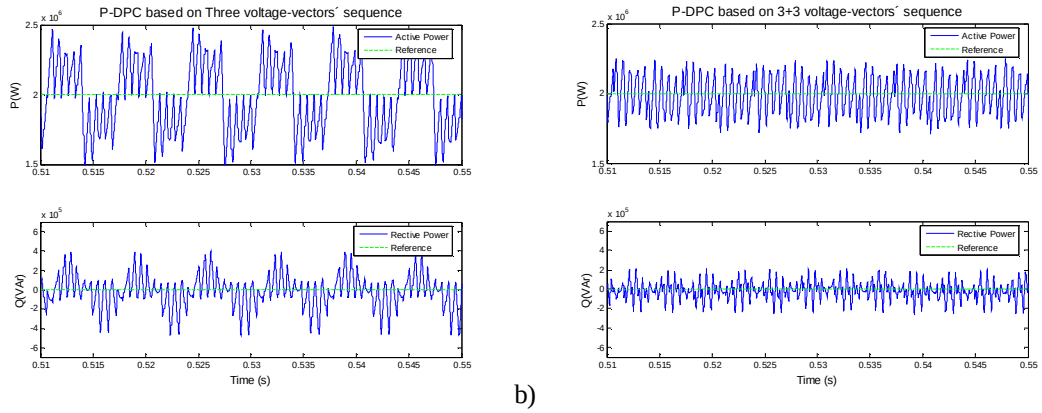
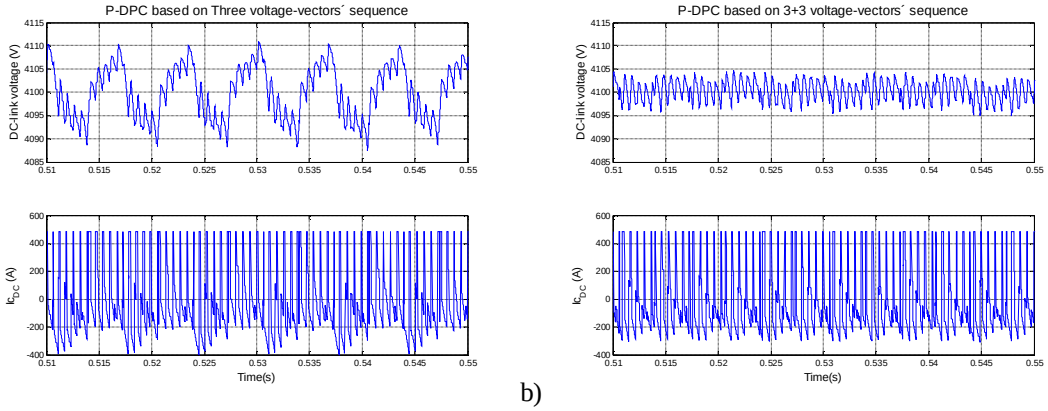


Fig.4.18: 2L-VSI. Phase switching signals, normalized line current and frequency spectrum: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence



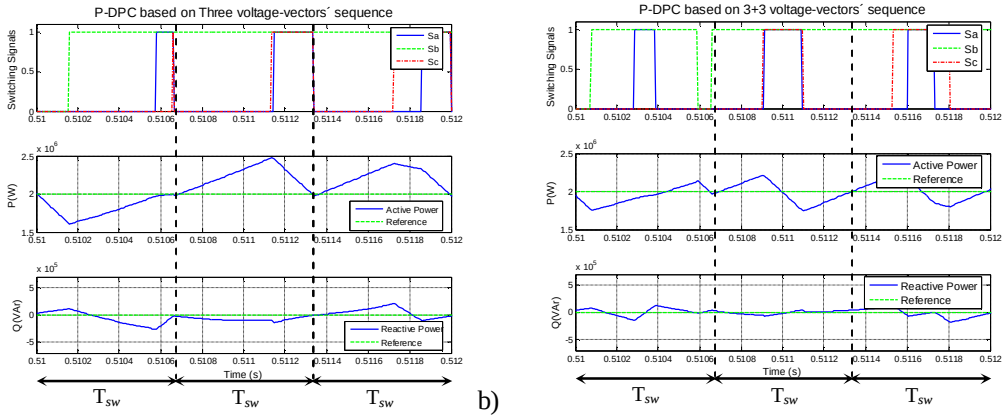
a) b)

Fig.4.19: 2L-VSI. Active and reactive power behaviors: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence



a) b)

Fig.4.20: 2L- VSI. DC-link voltage and capacitor's current ripple: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence



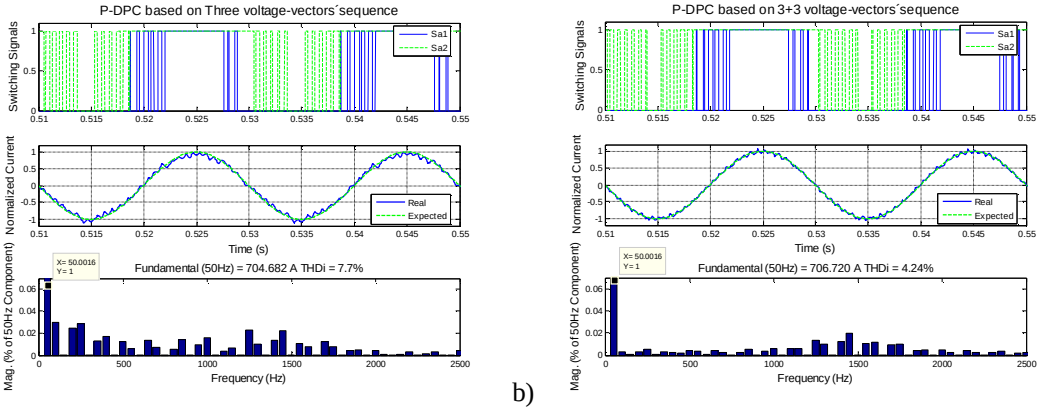
a) b)

Fig.4.21: 2L- VSI. Switching signals and active and reactive power trajectories along three control periods: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence

Finally, Fig.4.22 shows the resulting per-phase switching pattern, normalized line current and frequency spectrum for the 3L-NPC VSI under P-DPC versions based on simple 3 and symmetrical 3+3 voltage-vectors' sequence. As well as the last control algorithms, there are no switching actions during the line-current maximum, leading to minimum switching losses in the VSI. The THD measurements do not fulfill the IEEE Std. 519-1992 in the non-symmetrical P-DPC strategy (THDi= 7.7%). However, the symmetrical version meets this recommendation with a current THD of around 4.24%. This improvement involves frequency spectrum, power behavior and DC-link voltage ripple performances, see Fig.4.23 and Fig.4.24. This way, the active and reactive power ripples are reduced respectively from 14% and 9.81% for the simple sequence case to 7.35% and 5.42% for the symmetrical sequence case. Similarly, the DC-link voltage ripple decreases from 0.21% to 0.07% and the RMS current is kept at almost the same level (275A against 270A).

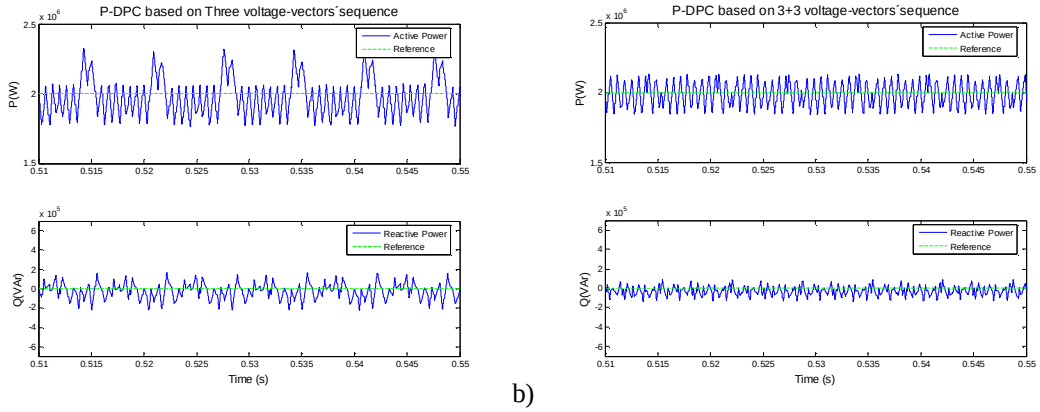
The absolute tracking error is near 0.74% in the non-symmetrical P-DPC strategy and close to 0.46% under its symmetrical version. Detailed behaviors of the relevant variables during three control periods are shown in Fig.4.25.

It should be noted that the non-symmetrical switching pattern produces a substantial disturbance in the line current maximum in steady state operation. This is a collateral effect related to the vectors' application sequence, also see Fig.4.18 and Fig.4.22.



a) b)

Fig.4.22: 3L-NPC VSI. Phase switching signals, normalized line current and frequency spectrum: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence



a) b)

Fig.4.23: 3L-NPC VSI. Active and reactive power behaviors: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence

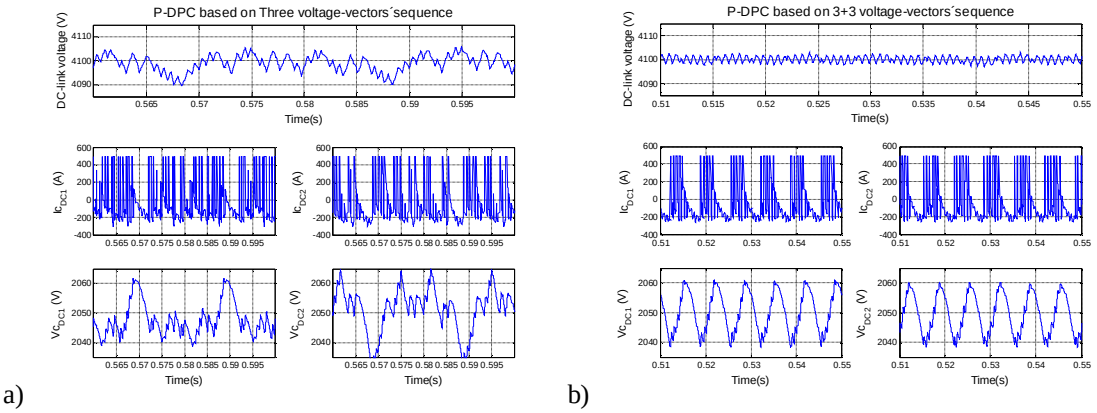


Fig.4.24: 3L-NPC VSI. DC-link voltage and capacitor's current ripple: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence

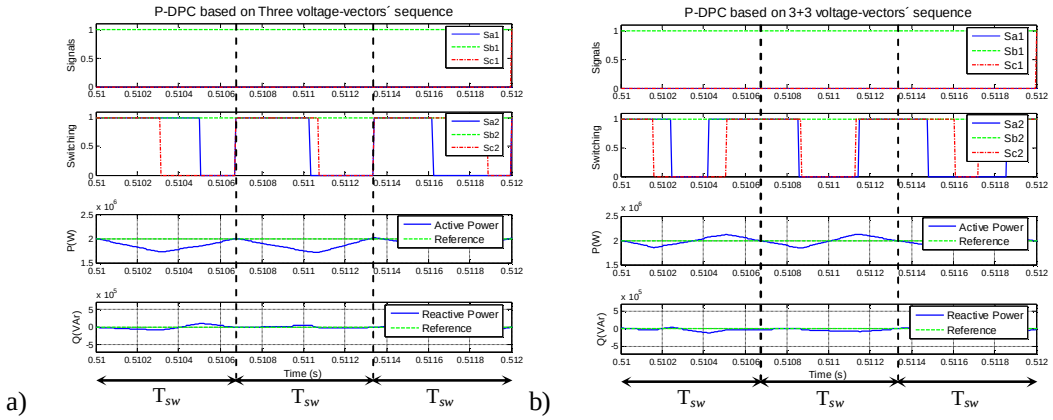
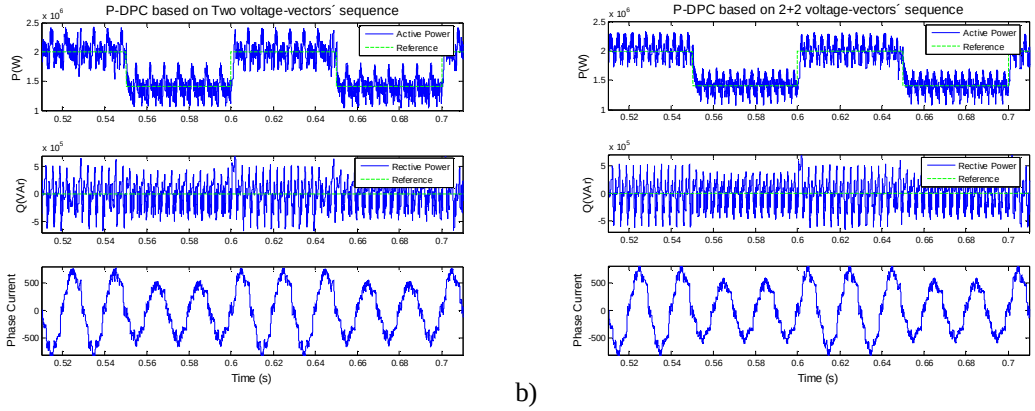


Fig.4.25: 3L- NPC VSI. Switching signals and active and reactive power trajectories along three control periods: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence

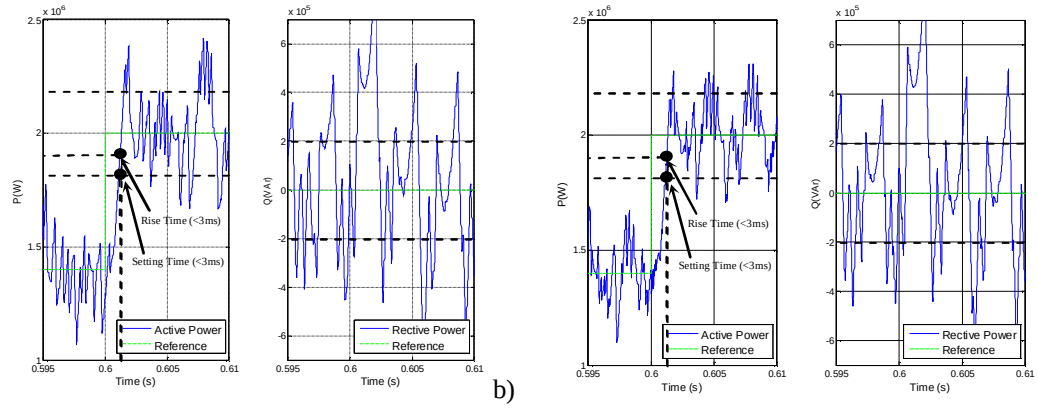
4.4.2. Transient Performance

Active power steps from 1.4MW to 2MW have been applied (power variations of 30%). Only active power changes are analyzed, though similar results can be obtained if reactive power steps are considered. Fig.4.26 shows the instantaneous active and reactive power behavior, involving the non-symmetrical and symmetrical two vectors-based P-PDC versions, when several active power reference steps are applied to the 2L-VSI. A fast transient response without overshoot and cross-coupling effect between variables is observed. Fig.4.27 shows the detail of the transient behavior. Considering a band of 10% of the nominal power, both P-DPC versions provide a setting time and rise time below 3ms. It can be concluded that both strategies provide the same dynamic performance. This equivalent behavior is due to the fact that both control strategies are under saturation during transients, i.e., the null vector is not applied and all the switching period is assigned to the same active vector, leading to the same transient evolution.



a) b)

Fig.4.26: 2L-VSI. Instantaneous active and reactive power behaviors during active reference steps: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence

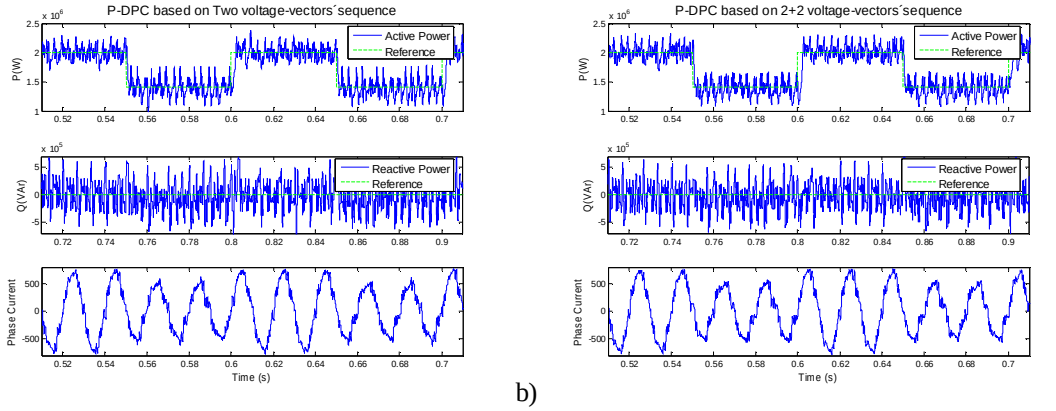


a) b)

Fig.4.27: 2L-VSI. Amplified active and reactive power transient behaviors: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence

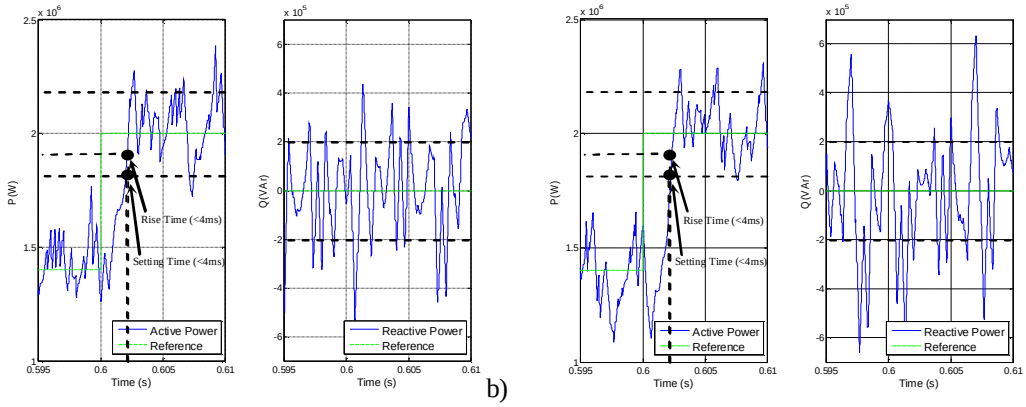
Several simulations of the 3L-NPC VSI under P-DPC based on simple 2 and symmetrical 2+2 voltage-vectors' sequences have been carried out, see Fig.4.28 and Fig.4.29. As well as previous strategies, a fast transient performance without overshoot and cross-coupling effects is observed. The rise time and setting time are around 4ms in both control algorithms.

Fig.4.30 describes the behavior of the active and reactive-power of the 2L-VSI during several active-power steps under P-DPC based on a simple 3 and symmetrical 3+3 switching patterns. The dynamic performance is similar in both techniques because the transient requirement leads to saturation of the control in such a way that the same voltage-vector is used along the entire switching period. There is no overshoot or cross-coupling effect, resulting on a rise time and setting time below 3ms. Similar results are obtained when the 3L-NPC VSI is considered, see Fig.4.32 and Fig.4.33.



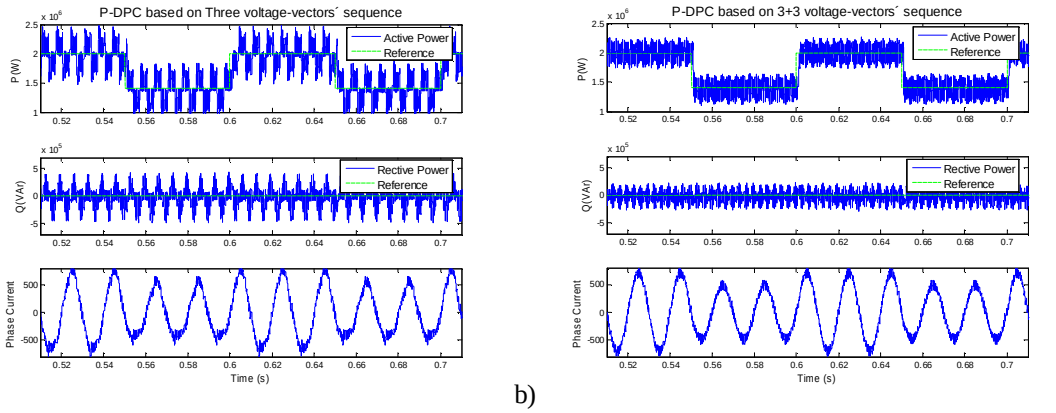
a) b)

Fig.4.28: 3L-NPC VSI. Instantaneous active and reactive power behaviors during active reference steps: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence



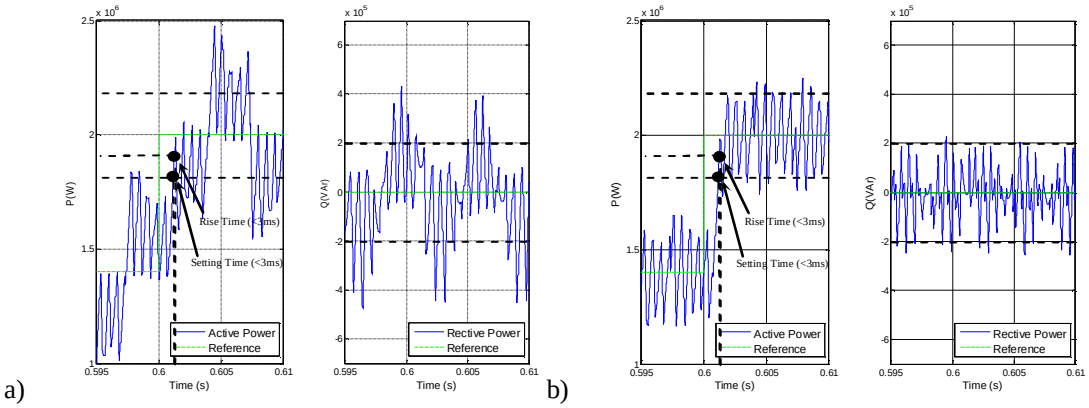
a) b)

Fig.4.29: 3L-NPC VSI. Amplified active and reactive power transient behaviors: a) P-DPC based on a two voltage-vectors' sequence, b) P-DPC based on a 2+2 voltage-vectors' sequence



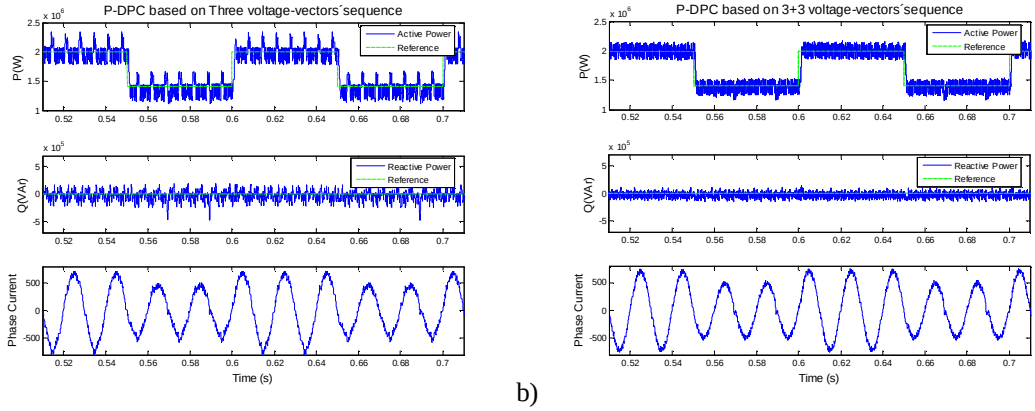
a) b)

Fig.4.30: 2L-VSI. Instantaneous active and reactive power behaviors during active reference steps: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence



a) b)

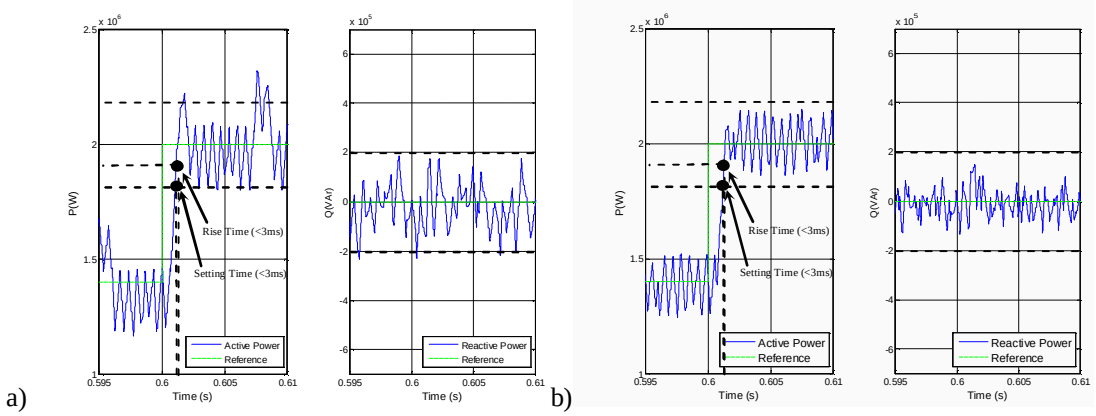
Fig.4.31: 2L-VSI. Amplified active and reactive power transient behaviors: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence



a)

b)

Fig.4.32: 3L-NPC VSI. Instantaneous active and reactive power behaviors during active reference steps: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence



a) b)

Fig.4.33: 3L-NPC VSI. Amplified active and reactive power transient behaviors: a) P-DPC based on a three voltage-vectors' sequence, b) P-DPC based on a 3+3 voltage-vectors' sequence

4.5. Conclusions

This Chapter has proposed a new predictive-type control algorithm based on the direct power control strategy, the P-DPC. Thanks to this new approach a constant-switching-frequency operation is obtained keeping the fast dynamic response related to direct control strategies. Different P-DPC versions, based on different voltage vectors' sequences, have been proposed and evaluated: simple 2 or 3 vectors' sequence and symmetrical 2+2 or 3+3 voltage vectors' sequences. Results have shown that the P-DPC could become an interesting alternative to MV grid-connected converters.

Table 4.2 and Table 4.3 show the simulation results along with the characteristics and requirements of each P-DPC version for the 2L-VSI and 3L-NPC VSI configurations. The results indicate that the symmetrical 3+3 switching-pattern establishes the best P-DPC version both in the 2L-VSI and 3L-NPC VSI configurations. Nevertheless, only the 3L-NPC VSI meets the IEEE Std 519-1992 recommendation which makes it an attractive choice for MV and high power applications.

TABLE 4.2
FEATURES AND REQUIREMENST OF P-DPC STRATEGIES FOR 2L-VSI

Features		**P-DPC based on two vectors**		**P-DPC based on three vectors**	
		Non-symmetrical switching pattern	**2+2 Symmetrical switching pattern**	**Non-symmetrical switching pattern**	**3+3 Symmetrical switching pattern**
Switching Frequency		Constant f_{swMAX} =3 kHz f_{Asw} =1kHz	Constant f_{swMAX} = 3 kHz f_{Asw} =1kHz	Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz	Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz
Control & Sampling Period		$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$
Modulation Technique		-	-	-	-
Steady-state	**Current THD**	14.75%	13.95%	13.85%	7.6%
	Tracking Error	0.87%	0.32%	0.86%	0.64%
	Power Ripple	ΔP (21.88%) ΔQ (33.44%)	ΔP (18.32%) ΔQ (33.74%)	ΔP (24.93%) ΔQ (20.88%)	ΔP (13.72%) ΔQ (11.86%)
	DC-link Ripple	Δv_{DC} (0.23%) Ic_{DCRMS}(277.11A)	Δv_{DC} (0.16%) Ic_{DCRMS}(276.42A)	Δv_{DC} (0.28%) Ic_{DCRMS}(281.29A)	Δv_{DC} (0.12%) Ic_{DCRMS}(273.71A)
Transient	**Cross-coupling Effect**	-	-	-	-
	Dynamic Performance	Setting time (<3ms) Rise time (<3ms) Overshoot (-)	Setting time (<3ms) Rise time (<3ms) Overshoot (-)	Setting time (<3ms) Rise time (<3ms) Overshoot (-)	Setting time (<3ms) Rise time (<3ms) Overshoot (-)

TABLE 4.3
FEATURES AND REQUIREMENST OF P-DPC STRATEGIES FOR 3L-NPC VSI

Features		**P-DPC based on two vectors**		**P-DPC based on three vectors**	
		Non-symmetrical switching pattern	**2+2 Symmetrical switching pattern**	**Non-symmetrical switching pattern**	**3+3 Symmetrical switching pattern**
Switching Frequency		Constant f_{swMAX} =3 kHz f_{Asw} =1kHz	Constant f_{swMAX} = 3 kHz f_{Asw} =1kHz	Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz	Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz
Control & Sampling Period		$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$
Modulation Technique		-	-	-	
Steady-state	**Current THD**	13.59%	12.67%	7.7%	4.24%
	Tracking Error	0.73%	0.26%	0.74%	0.46%
	Power Ripple	ΔP (21.75%) ΔQ (36.42%)	ΔP (15.23%) ΔQ (33.34%)	ΔP (13.95%) ΔQ (9.81%)	ΔP (7.35%) ΔQ (5.42%)
	DC-link Ripple	Δv_{DC} (0.23%) Ic_{DCRMS}(277.43A)	Δv_{DC} (0.17%) Ic_{DCRMS}(276.95A)	Δv_{DC} (0.21%) Ic_{DCRMS}(275.50A)	Δv_{DC} (0.07%) Ic_{DCRMS}(270.13A)
Transient	**Cross-coupling Effect**	-	-	-	-
	Dynamic Performance	Setting time (<4ms) Rise time (<4ms) Overshoot (-)	Setting time (<4ms) Rise time (<4ms) Overshoot (-)	Setting time (<3ms) Rise time (<3ms) Overshoot (-)	Setting time (<3ms) Rise time (<3ms) Overshoot (-)

Chapter 5

5. Control Operation Performance

5.1. Introduction

It is important to know the behavior of any control algorithm when several non-considered real-world phenomena are present, e.g. a non accurate estimation of parameters. In the same way, the control strategies proposed in this dissertation must face up to regulation tasks which are mainly required by two types of disturbances: line-voltage harmonics and sags.

Firstly, this chapter summarizes the non-perturbed performances of the proposed control algorithms. Secondly, it is studied the operation of the proposed control strategies under balanced inductance-drifts. Finally, the behavior of the control algorithms during disturbed conditions is analyzed. This last feature is commonly denoted as the regulation capability.

5.2. Features and Specifications of the Control Operation Performance

Table 5.1 compares the main features and specifications of the most interesting control algorithms developed and analyzed in Chapter 3 and Chapter 4. As can be observed, all control strategies operate at the same switching frequency, with identical control and sample periods. Therefore, a coherent comparative frame can be considered and different conclusions are derived.

For a given converter, all the control strategies show almost the same current THD levels, near 8% in the 2L-VSI and around 4.25% in the 3L-NPC VSI. However, the power and DC-voltage ripples are lower in the P-DPC case and the absolute current tracking error is smaller when VOC-based strategies are utilized. These results are coherent with the fact that the main aim of the P-DPC is to minimize the active and reactive power error, whereas the minimization of current error is considered in the VOC-type strategies.

The transient behavior shows a *d-q* cross-coupling effect between control variables when VOC techniques are used. The design characteristics of the P-DPC algorithm make it non susceptible toward this effect. Anyway, the best P-DPC results, as expected, are obtained in the dynamic performances. It is clearly faster in the power tracking task in both configurations, as it takes less than 3ms instead of around 16ms required by the VOC strategies. Furthermore, the P-DPCs establish the fastest rise time below 3ms without overshoot, whereas the VOCs employs around 8ms with considerable overshoot. Therefore it can be said that the P-DPC is an attractive choice for MV grid-connected applications.

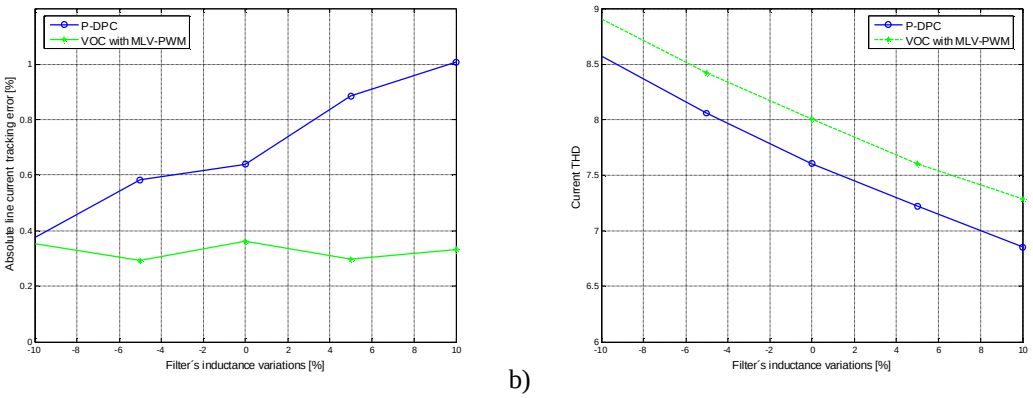
TABLE 5.1
FEATURES AND SPECIFICATIONS

Features		2L-VSI		3L-NPC VSI	
		VOC with MLV-PWM	**P-DPC based on a symmetrical 3+3 switching pattern**	**VOC with NTV-SVM**	**P-DPC based on a symmetrical 3+3 switching pattern**
Switching Frequency		Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz	Constant f_{swMAX} = 1.5 kHz f_{Asw} =1kHz	Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz	Constant f_{swMAX} =1.5 kHz f_{Asw} =1kHz
Control & Sampling Period		$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$	$T_{sw}=1/f_{swMAX}$
Modulation Technique		MLV-PWM	-	NTV-SVM	-
Steady-state	**Current THD**	8%	7.6%	4.26%	4.24%
	Tracking Error	0.36%	0.64%	0.37%	0.46%
	Power Ripple	ΔP (12.37%) ΔQ (14.96%)	ΔP (13.72%) ΔQ (11.86%)	ΔP (9.15%) ΔQ (8.27%)	ΔP (7.35%) ΔQ (5.42%)
	DC-link Ripple	Δv_{DC} (0.14%) Ic_{DCRMS}(274.56A)	Δv_{DC} (0.12%) Ic_{DCRMS}(273.71A)	Δv_{DC} (0.11%) Ic_{DCRMS}(272.34)	Δv_{DC} (0.07%) Ic_{DCRMS}(270.13A)
Transient	**Cross-coupling Effect**	Yes	-	Yes	-
	Dynamic Performance	Setting time (<16ms) Rise time (<8ms) Overshoot (~5%)	Setting time (<3ms) Rise time (<3ms) Overshoot (-)	Setting time (<15ms) Rise time (<8ms) Overshoot (~8%)	Setting time (<3ms) Rise time (<3ms) Overshoot (-)

5.3. Filter's Inductance Variations

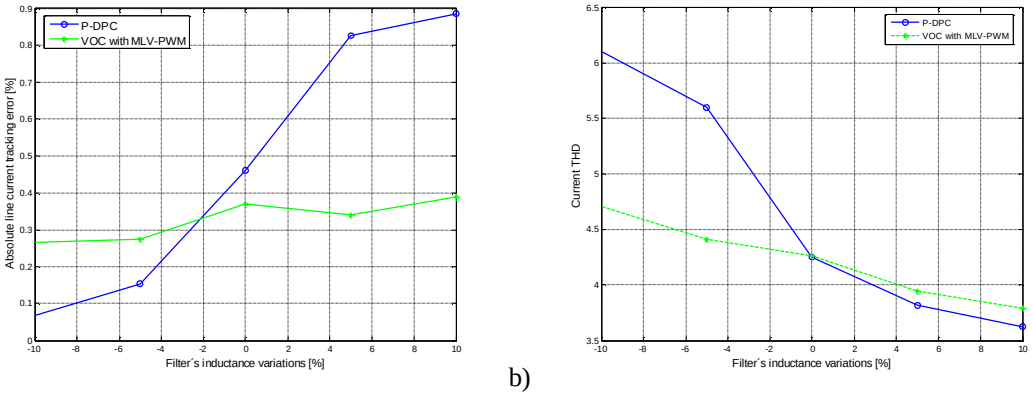
The line-filter's inductance variations could affect the performance of the grid-connected converter [13;43]. The VOC-based strategies are reasonably insensitive to these variations that only affect the current's spatial-orientation related to the line-voltage phase estimation. Therefore, an influence in the power factor can be induced but it is usually corrected by the current control loop. On the other hand, the P-DPC is a model based control method, so its mathematical approach is based on the knowledge of the system's parameters, becoming sensitive to parameter drifts. A deviation in the filter's inductance could damage the stability of the control system. Fig.5.1 and Fig.5.2 show the absolute line current tracking error and the influence on THD when a typical derivation of 10% in the filter's inductance is produced.

As can be observed, a deviation in the inductance produces small errors in the power tracking when VOC-based techniques are employed. The deviation of 10% in the inductance value will imply an absolute power tracking error below 1% both in the 2L-VSI and in the 3L-NPC VSI, which does not damage the stability of the control system performance. Yet, it can produce significant variations in THD measurements under the 3L-NPC VSI, which implies that this configuration is very sensitive to filter's inductance variations.



a) b)

Fig. 5.1: 2L-VSI. Filter inductance variations: a) Absolute power tracking error, b) Current THD measurements



a) b)

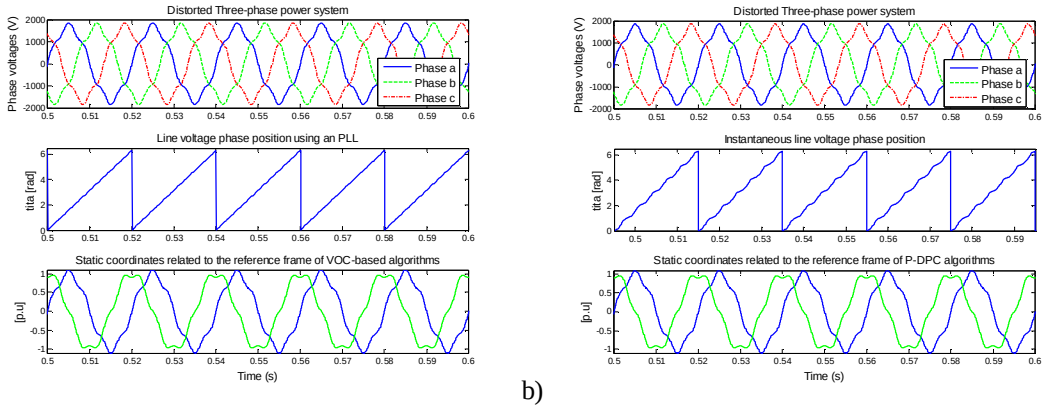
Fig.5.2: 3L-NPC VSI. Filter inductance variations: a) Absolute power tracking error, b) Current THD measurements

5.4. Power Quality Disturbances

The ideal characteristics of power energy in the generation point can be modified during the transport and distribution operations or by the customers [12;14;15;113-116]. The drift of any ideal grid parameter is denoted as electrical disturbance. Under ideal conditions the VSIs should provide sinusoidal line currents but a distorted grid voltage can induce a negative effect in the converter's performance. It is so interesting to evaluate the influence of these perturbations on the proposed control algorithms

5.4.1. Influence of Line-voltage Harmonics

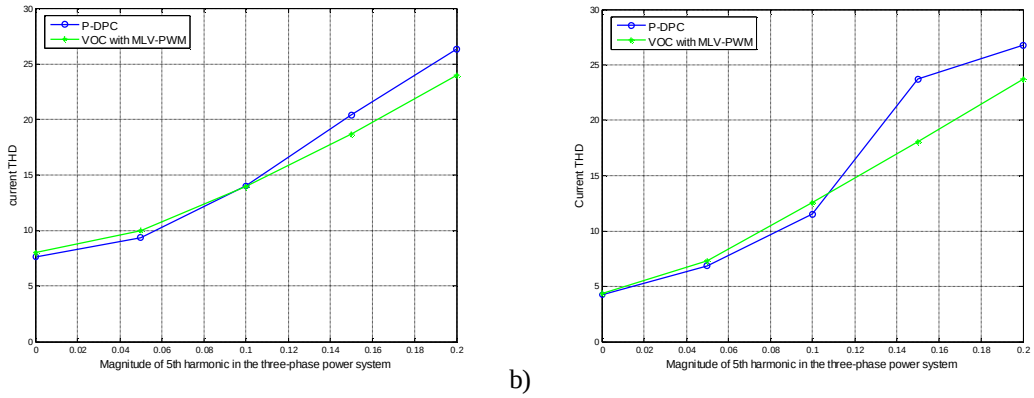
In an ideal situation, the grid usually consists of a balanced three-phase power system with sinusoidal line voltage-waves. However, the line voltage is frequently distorted and the systems which are connected to the grid should be able to tolerate this situation [43;117;117-119]. One of the main disturbances is the presence of line voltage harmonics of order 5, 7 and 11. Fig.5.3 shows the influence in the proposed control algorithms when a balanced 5^{th} voltage of 10% appears. The VOC-based strategies usually employ a PLL in order to obtain the line voltage phase position, so these control techniques show a good performance against line voltage harmonics, see Fig.5.3a. On the other hand, the P-DPC is based on the instantaneous line voltage phase estimation and the disturbances affect the control performance directly, see Fig.5.3b.



a) b)

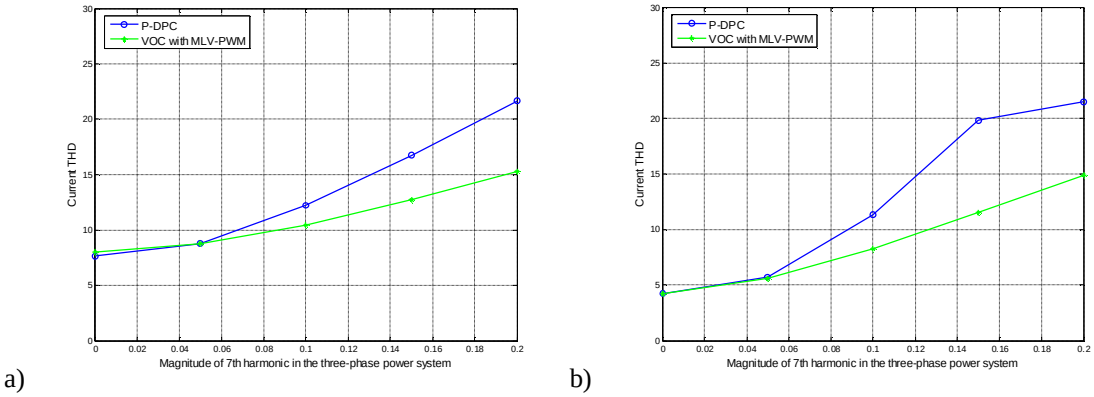
Fig.5.3: Influence in the control algorithm when a 10% of 5^{th} voltage harmonic is applied: a) VOC-based strategies, b) P-DPC-based strategies

Fig.5.4, Fig.5.5 and Fig.5.6 show several current THD values, both in the 2L and 3L-NPC VSI configurations, in presence of different magnitudes of 5^{th}, 7^{th}, and 11^{th} line voltage harmonics. These figures describe a generalized trend which implies an increase of current-THD according to the magnitude of line-voltage harmonic. As expected, the P-DPC-based algorithms have a higher sensitivity to these disturbances.



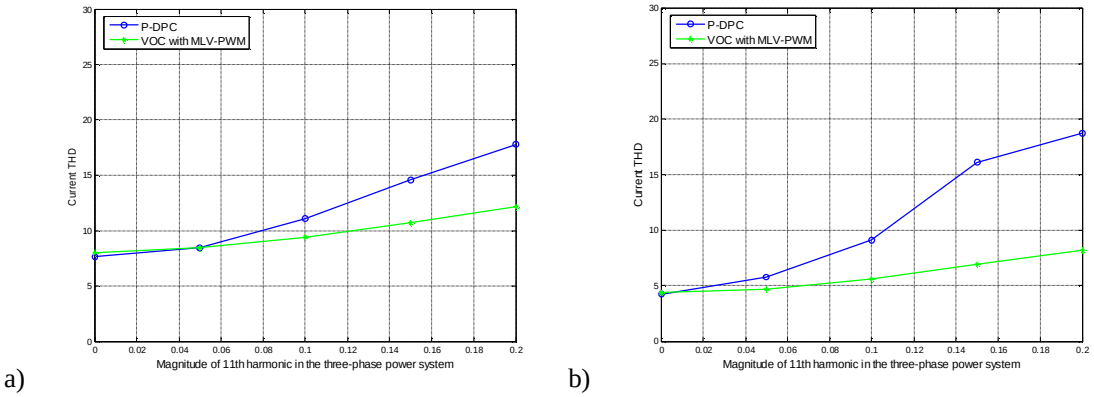
a) b)

Fig.5.4: Current THD measurements in presence of 5^{th} voltage harmonic: a) 2L-VSI, b) 3L-NPC VSI



a) b)

Fig.5.5: Current THD measurements in presence of 7th voltage harmonic: a) 2L-VSI, b) 3L-NPC VSI



a) b)

Fig.5.6: Current THD measurements in presence of 11th voltage harmonic: a) 2L-VSI, b) 3L-NPC VSI

5.4.2. Influence of Line-voltage Sags

The voltage sag could be defined as a strong drop in line-voltage (between 10% and 90% of nominal value) during a short period of time which is usually established between 10ms and 1min. These kind of disturbances are typically originated by short-circuits and grid connection/disconnection of large loads (transformers, motors and others) within the distribution power system [12;13;120-122]. An interesting classification of line voltage sags has been recently presented in [13]. This dissertation discusses the results of several grid measurements in the distribution power systems which have been carried out by a Spanish utility company between 1997 and 2000. As a result, it could be derived that around 80% of grid faults are related to voltage sags below 50% and lasting less than 200ms. Fig.5.7 shows the main characteristics of some of the most common line-voltage sags which can be generated in the electrical power system. Thus, the A case represents a balanced three-phase voltage sag. The B case shows a single-phase voltage sag and C and D cases describe different two-phase voltage-sags. Here, $\vec{V}$ is the perturbed line-voltage whereas $\vec{F}$ is used for non-perturbed phase.

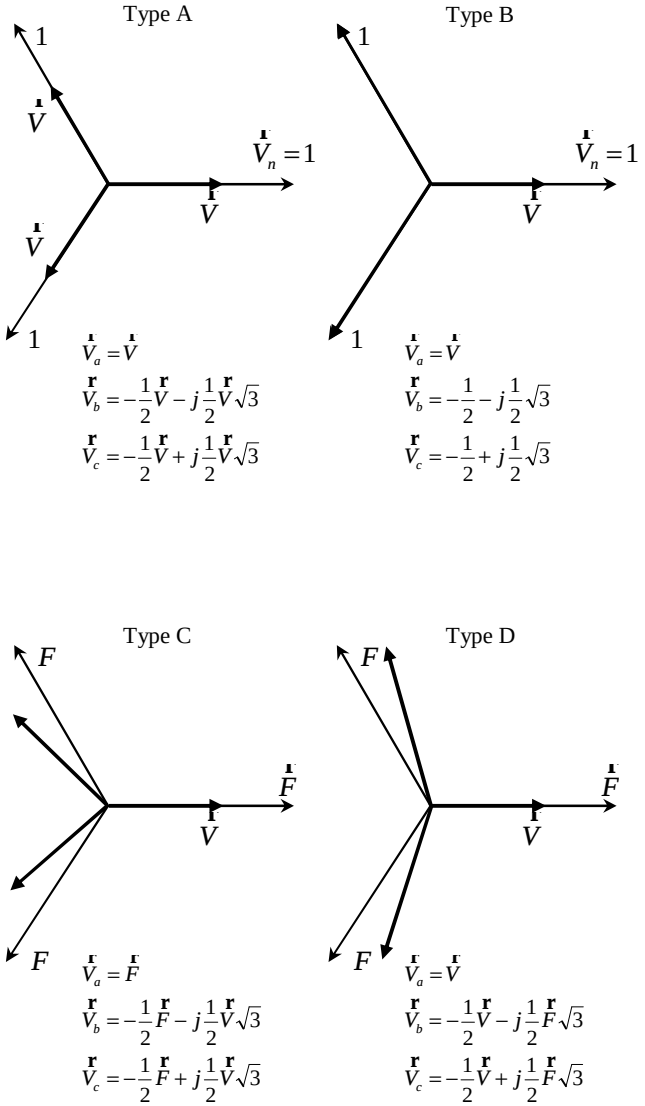
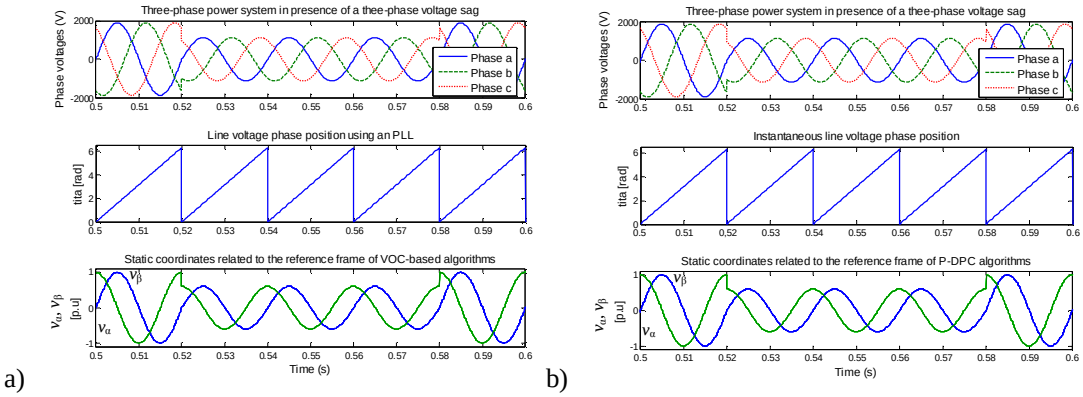


Fig.5.7: Phasor-diagram-based classification of line voltage sags (p.u)

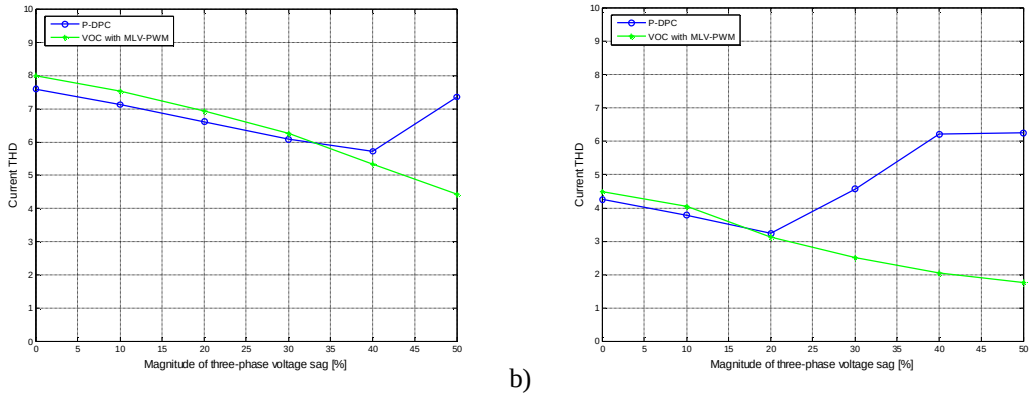
From the point of view of the proposed VOC strategies, the voltage sag induces a disturbance in the current loop which tends to evolve toward the new current requirements which are established by the DC regulation loop. In the P-DPC algorithm, the line voltage sag directly leads to a proportional increase of line current in order to keep the power requirements constant. Fig.5.8 shows the line-phase estimation of the VOC and P-DPC algorithms in the presence of a three-phase voltage sag (type A) between 0.52s and 0.58s. Both control algorithms show a similar behavior which is coherent with the fact that the three-phase balance is kept during the voltage drop.



a) b)

Fig.5.8: Influence of a three-phase voltage sag in the control algorithm (*V*=40%): a) VOC-based strategies, b) P-DPC-based strategies

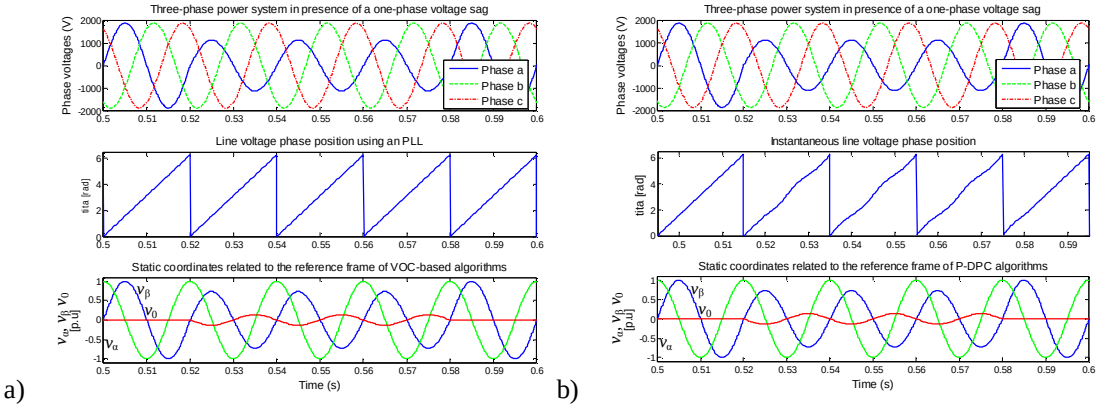
Fig.5.9 shows several current THD measurements in presence of different magnitudes of three-phase voltage sags. These results are obtained keeping the power reference during the disturbed conditions. As a result, an increase in the magnitude of line voltage sag involves larger line currents, which decreases the current THD. The VOC-based strategies follow this trend, but substantial voltage sags has an effect on the performance of the VSI when the P-DPC is employed. In fact, voltage-sags over 35% increase the THD levels on the 2L-VSI in relation to the VOC strategy, whereas this limit falls down to 20% on the 3L-NPC VSI case. Therefore, the P-DPC-based algorithms are sensitive to three-phase voltage sags, becoming the 3L-NPC VSI the weakest configuration.



a) b)

Fig.5.9: Current THD measurements in presence of different three-phase voltage sags: a) 2L-VSI, b) 3L-NPC VSI

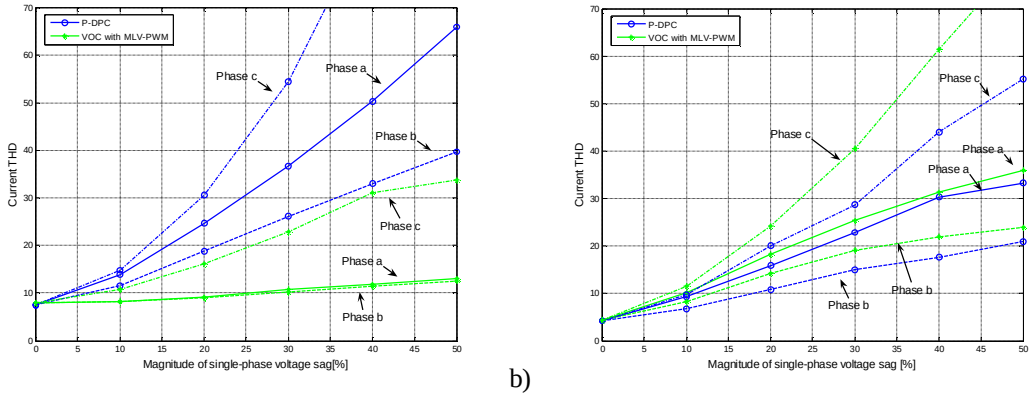
Fig.5.10 describes the influence of a single-phase voltage sag (type B) between 0.52s and 0.8s. It is interesting to observe that the zero sequence of the static reference frame v_0 shows a significant variation during the perturbed conditions. However, the PLL system keeps the line phase estimation free of perturbations in the VOC strategies in such a way that the control variables can operate under an undisturbed reference. On the other hand, the line voltage sag clearly affects the P-DPC algorithm, leading to instantaneous grid phase deviation.



a) b)

Fig.5.10: Influence of a one-phase voltage sag in the control algorithm (*V*=40%): a) VOC-based strategies, b) P-DPC-based strategies

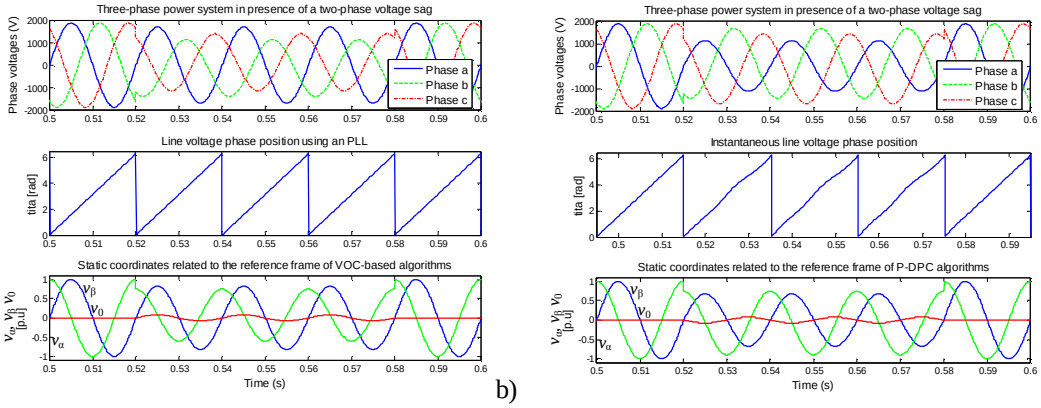
In the same way as in the three-phase voltage sag analysis, it is possible to compute the current THD values when different single-phase voltage sags are applied, see Fig.5.11. The results of the 2L-VSI show that the P-DPC is more sensitive than the VOC strategy in the presence of one-phase voltage sags. Nevertheless, this results differs in the 3L-NPC VSI case, where very sensitive behavior is observed under both control algorithms.



a) b)

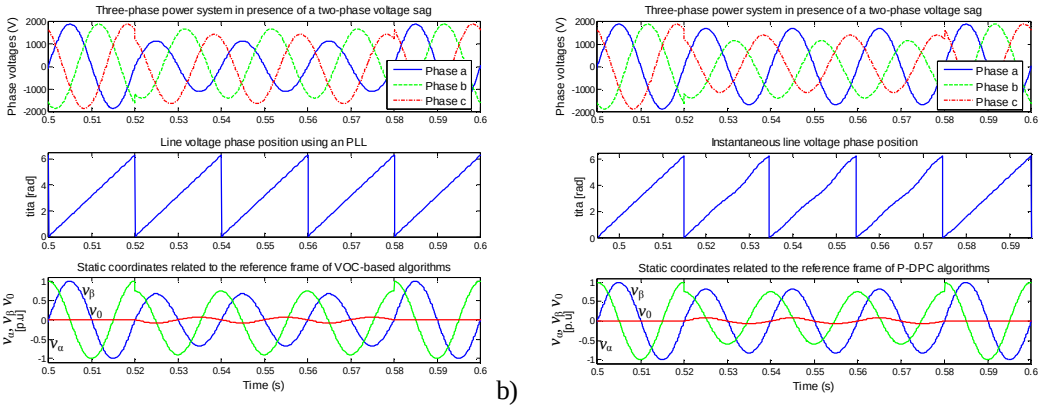
Fig.5.11: Current THD measurements in presence of different one-phase voltage sags: a) 2L-VSI, b) 3L-NPC VSI

Finally, the influence of the two-phase voltage sags is shown in Fig.5.12 and Fig.5.13. These results are related to C and D-type voltage sags which are described in Fig.5.7. The control performance is similar to the one-phase voltage sag disturbance situation, where unbalanced operation conditions are produced. Similarly to the previous cases, the PLL system keeps the line-phase estimation free of perturbations in the VOC strategies, whereas instantaneous variations are observed in the P-DPC algorithm.



a) b)

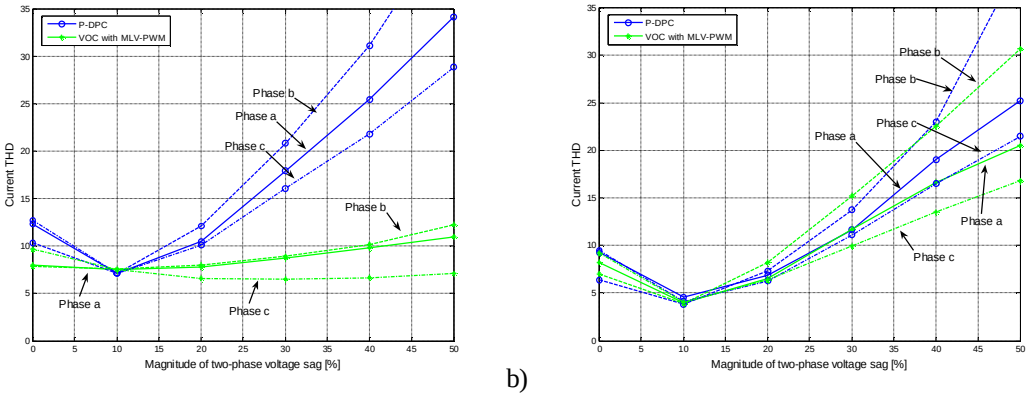
Fig.5.12: Influence of a two-phase voltage sag (type C) in the control algorithm (*V*=40%, *F*=10%): a) VOC-based strategies , b) P-DPC-based strategies



a) b)

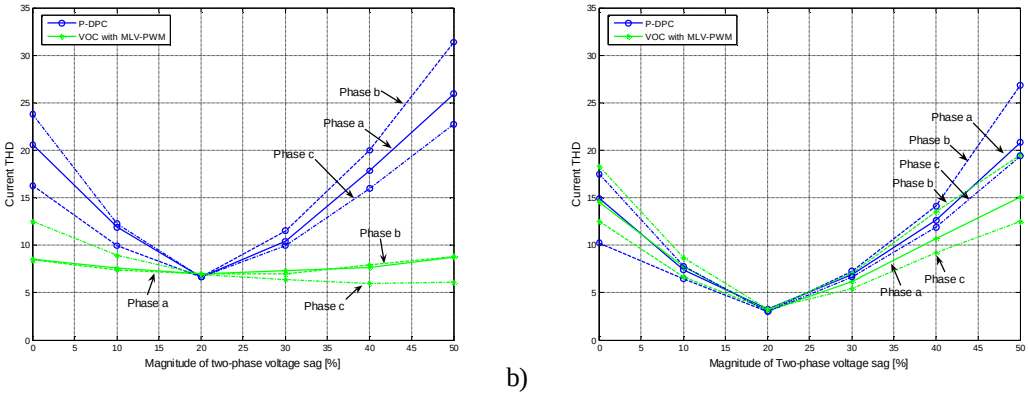
Fig.5.13: Influence of a two-phase voltage sag (type D) in the control algorithm (*V*=40%, *F*=10%): a) VOC-based strategies , b) P-DPC-based strategies

In order to show the influence of the two-phase voltage sags under the 2L and 3L-NPC VSIs several THD measurements under different voltage-sag conditions have been carried out. Fig.5.14 and Fig.5.15 show two situations related to different voltage drops in the non-affected grid-phase (*F*=10% and *F*=20%) for a C-type voltage sag. In a similar way, Fig.5.16 and Fig.5.17 describe the systems' behavior related to the same voltage drops in the non affected grid-phase for a D-type voltage sag. In the 2L-VSI, the current THD of the P-DPC case increases faster than in the VOC case when the magnitude of voltage sags moves away from the balanced situation. In the 3L-NPC VSI case, both control algorithms show a similar behavior with high variations in the systems' performance. As a result, the P-DPC algorithm is more sensitive than the VOC in the 2L-VSI case but the 3L-NPC VSI becomes a vulnerable configuration for both control strategies.



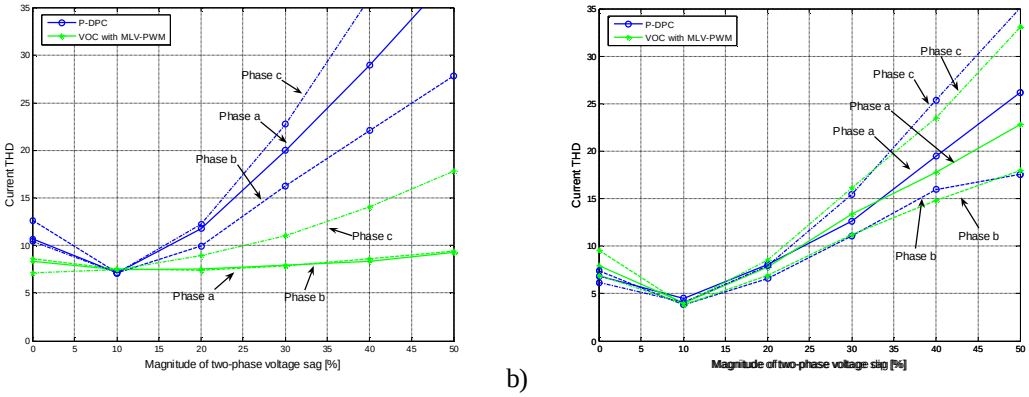
a) b)

Fig.5.14: Current THD measurements in presence of different two-phase voltage sags (*F*=10%): a) 2L-VSI, b) 3L-NPC VSI



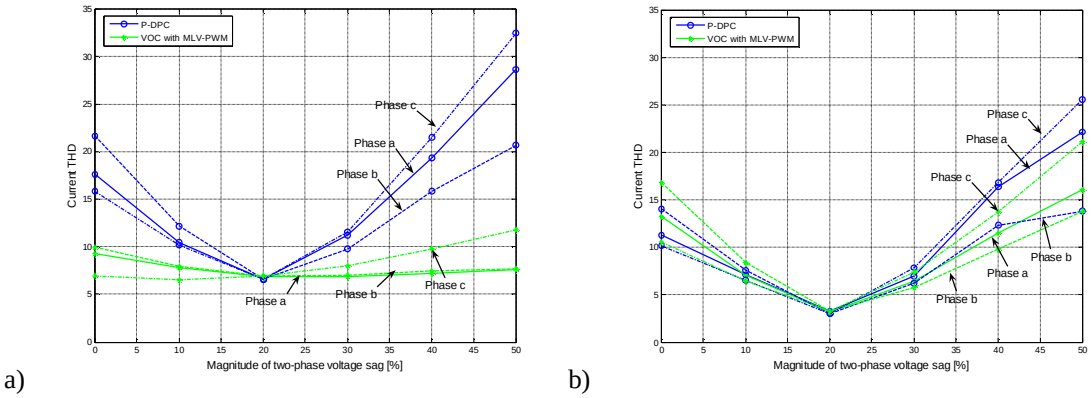
a) b)

Fig.5.15: Current THD measurements in presence of different two-phase voltage sags (*F*=20%): a) 2L-VSI, b) 3L-NPC VSI



a) b)

Fig.5.16: Current THD measurements in presence of different two-phase voltage sags (*F*=10%): a) 2L-VSI, b) 3L-NPC VSI



a) b)

Fig.5.17: Current THD measurements in presence of different two-phase voltage sags (*F*=20%): a) 2L-VSI, b) 3L-NPC VSI

5.5. Conclusions

A performance comparison between the previously selected control algorithms for MV grid-connected 2L and 3L-NPC VSIs has been carried out in this Chapter. Thus, VOC-type strategies based on MLV-PWM and NTV-SVM are compared with the P-DPC strategy based on symmetrical 3+3 voltage vectors' sequence. Furthermore, several important operation cases such as the influence of the filter's inductance deviations and some grid disturbances are discussed.

The control performance comparison shows that the P-DPC is an interesting alternative to standard VOC techniques for grid-connected converters. It shows high transient capabilities with a comparable power quality toward VOC strategies in the steady-state performance under a constant switching frequency. Nevertheless, it has been shown that the filter's inductance drifts of around 10% could affect the current tracking error. In spite of this, this value is established below 1% and it does not damage the stability of the control system in the 2L-VSI configuration. However, the 3L-NPC VSI is very sensitive to filter's parameter drifts whatever control is used.

The analysis of the influence of line voltage harmonics shows that P-DPC algorithms are considerably affected as harmonics magnitude and frequency levels increase. In a similar way, the P-DPC is very sensitive to the voltage sags. The VOC techniques are also affected by these perturbations and especially in the 3L-NPC VSI configuration when unbalanced operation conditions are produced.

Chapter 6

6. Experimental Results

6.1. Introduction

Experimental tests have been carried out in order to validate the proposed P-DPC algorithm. Three laboratory set-ups have been utilized: two different 2L-VSIs and one 3L-NPC VSI. As the laboratory set-ups are not high-power devices, none of them has a parameter's set similar to that resulting from the design considerations of Chapter 3. Because of that, data obtained from experimental tests will be compared with data derived from new simulations related to the new laboratory VSIs. The 3+3 vector's sequence and the hybrid version have been employed on the experimental test of the P-DPC.

6.2. Laboratory Set-ups

On the one hand, some of the experiments have been carried out at the Institute of Control & Industrial Electronics from Warsaw University of Technology (Poland). These experiments are related to a 2L-VSI operating as a rectifier. On the other hand, other experiments have been achieved at the Power Electronics Laboratory at the Faculty of Engineering of the University of Mondragon (Spain). These experiments compare the behavior of 2L and 3L-NPC VSI when different control strategies as the P-DPC and VOC-ones are used.

6.2.1. The 2L-VSI Operating as a Rectifier under the P-DPC

The experimental platform consists of a commercial three-phase inverter controlled by a dSPACE ds1103 real time platform, a line inductor of 10mH, a DC-link capacitor of 470μF and a resistor of 100Ω as passive load, see Fig.6.1. The main parameters of the power and control systems are listed in Table 6.1.

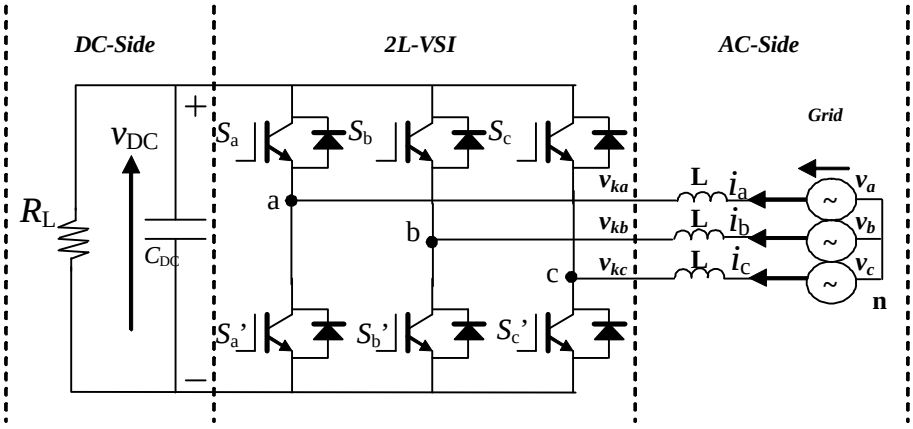


Fig.6.1: Electrical diagram. Laboratory platform of three-phase 2L-VSI with a L-type filter under rectifier operation mode

TABLE 6.1
SPECIFICATIONS OF POWER AND CONTROL SYSTEMS

	Value [unit]
Rated Power	**2.5 [kW]**
Rated line-to-line Voltage (RMS)	**260 [V]**
Filter	**L=10 [mH] R=100[mΩ]**
DC Link (C_{DC})	**470 [mF]**
Resistive Load	**R_L=100[Ω]**
P-DPC based on 3+3 voltage vectors' sequence	
Switching Frequency (maximum)	**f_{swMAX}=7500[Hz]**
Control & Sample	**$T_{sw}=1/f_{swMAX}$**

As shown in Chapter 3, in the beginning of each control period the P-DPC algorithm computes active and reactive powers based on the instantaneous current and voltage measures. Next, it selects the optimal voltage vectors' sequence and the related application times, taking into account the power tracking requirements. The control task takes few μs, which are negligible against the control period. After this short delay time, the selected voltage vectors are applied during the computed application times, completing the control period. The control algorithm (instantaneous power derivation, vectors' sequence selection and computing of the application times) runs under an integrated ControlDesk program in a dSPACE ds1103 real time platform. As the space vector modulation facility of this platform is not flexible enough, the desired switching patterns are "coded" using scalar PWM facilities. The desired actual voltage-vector sequence is finally generated "decoding" these standard PWM outputs by combinatory logic circuits. The measurement system is based on a TEKTRONIX TDS3014 100MHz oscilloscope and a grid analyzer NORMA D6000 (Goerz Instruments).

Initial steady-state tests have been carried out on a 2L-VSI operating at 150V/2kW. Fig.6.2 shows the simulated and experimental per-phase grid-voltage, line-current and the converter's voltage related to the negative point of the DC-link. As it can be derived, there are no switching actions along the maximum of the line current, minimizing the overall switching losses.

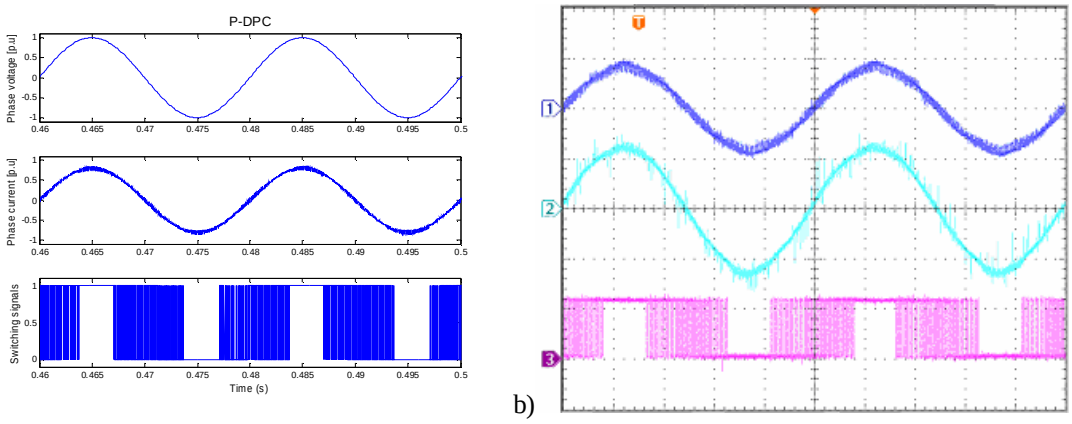


Fig.6.2: a) Simulated per-phase grid voltage, line current and converter's per-phase switching signals under normalized values (p.u), b) Experimental per-phase grid voltage, line current and per-phase converter's voltage related to negative point of the DC-link

Oscilloscope: From the top grid voltage 250V/div, line current 5A/div and converter's voltage 400V/div (time division of 4ms)

This efficiency improvement is related to current spectrum-deterioration, as it will be shown next. The grid-voltage and current-frequency spectrum are computed taking into account the average value over 16 grid periods, see Fig.6.3and Fig.6.4. The current THD measurements show a very good power quality (THD_i=2.87%), whereas a deterioration of the grid-voltage is observed (THD_v=2.71%). In spite of this, the overall behavior meets the IEEE Std 519-1992 recommendation.

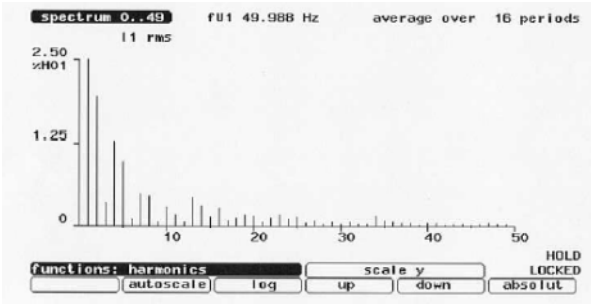


Fig.6.3: Experimental current frequency spectrum

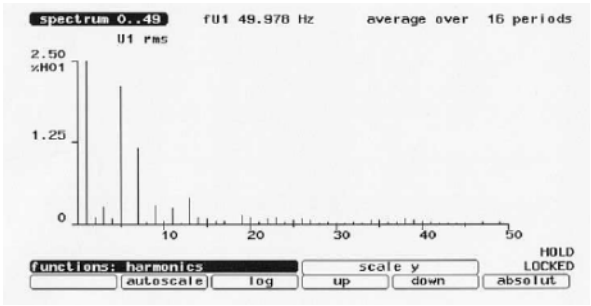


Fig.6.4: Experimental voltage frequency spectrum

Very good results are also obtained in transient behavior, see Fig.6.5. Active power reference steps from 1.5kW to 2.5kW have been applied. As can be observed on Fig.6.6, the P-DPC transient takes around 400µs without overshoot and a negligible cross-coupling effect. The behavior of the line-current and converter's voltage related to the negative point of the DC-link are shown in Fig.6.7.

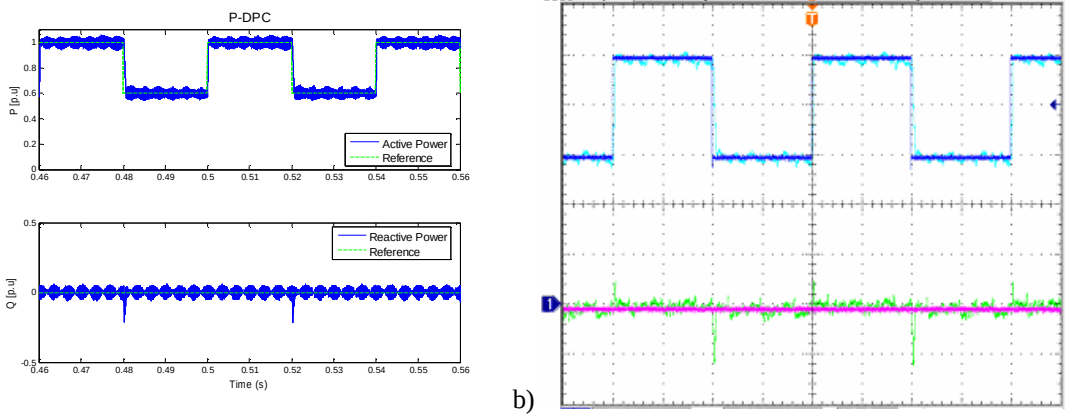


Fig.6.5: Instantaneous active and reactive power behaviors during active reference steps: a) Simulated Results (normalized values), b) Experimental results

Oscilloscope: From the top reference & active power 500W/div and reference & reactive power 200W/div (time division of 10ms)

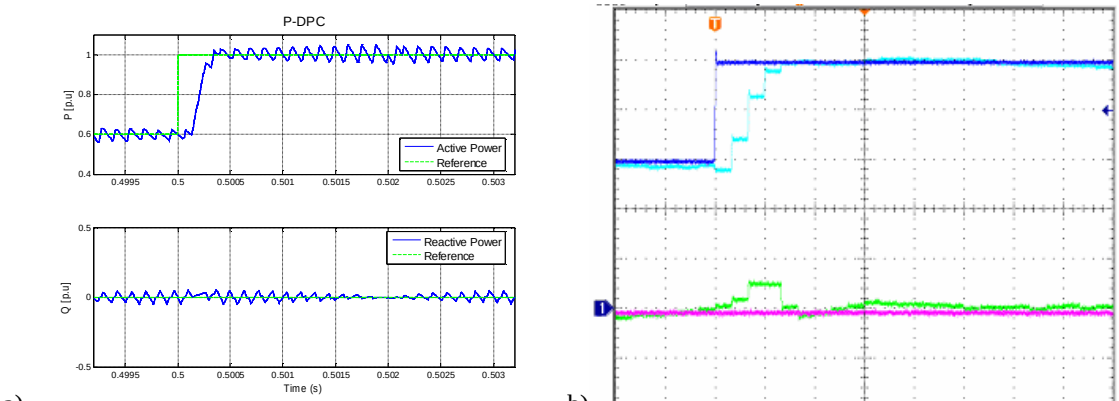


Fig.6.6: Amplified instantaneous active and reactive power behaviors during active reference steps: a) Simulated Results (normalized values), b) Experimental results

Oscilloscope: From the top reference & active power 500W/div and reference & reactive power 200W/div (time division of 400µs)

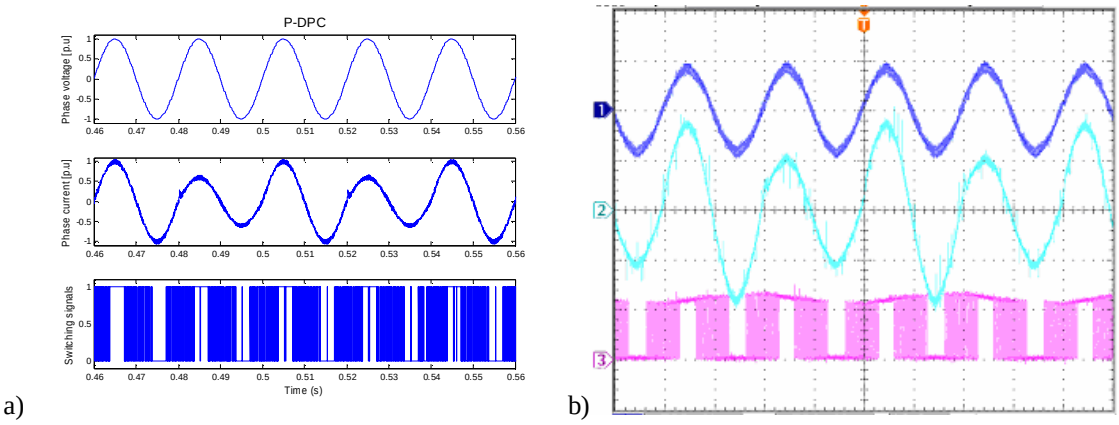


Fig.6.7: a) Simulated per-phase grid voltage, line current and converter's per-phase switching signals under normalized values, b) Experimental per-phase grid voltage, line current and per-phase converter's voltage related to negative point of the DC-link

Oscilloscope: From the top grid voltage 250V/div, line current 5A/div and converter's voltage 400V/div (time division of 10ms)

6.2.2. Comparative Study of the P-DPC and the VOC Strategies on a 2L-VSI Operating as an Inverter

The symmetrical 3+3 vectors' sequence version of the P-DPC and VOC strategies have been compared on a grid-connected three-phase VSI operating at 400V-15kVA. The experimental platform consists of a commercial three-phase inverter SKITPPACT (SEMIKRON), a line inductor of 10mH, a DC-link capacitor of 5mF and a DC supply source, see Fig.6.8. The main specifications of power and control systems are listed in Table 6.2.

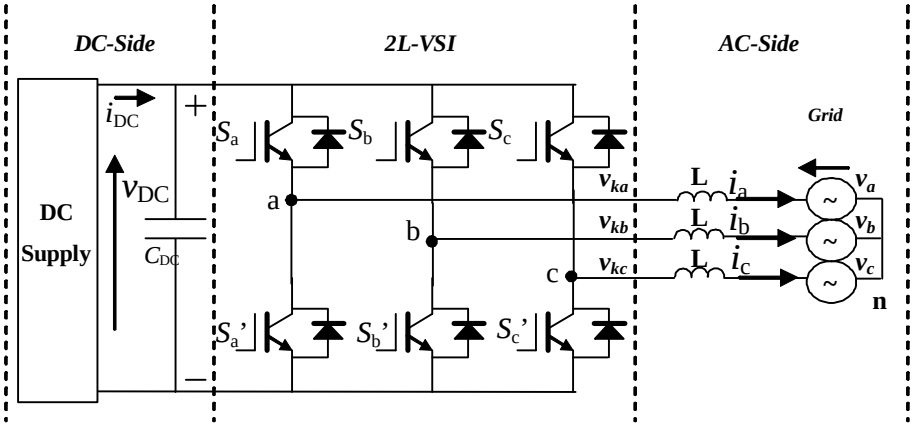


Fig.6.8: Electrical diagram. Laboratory platform of three-phase 2L-VSI with a L-type filter under rectifier operation mode

TABLE 6.2
SPECIFICATIONS OF POWER AND CONTROL SYSTEMS

	Value [unit]
Rated Power	**15 [kVA] cosθ=0.8 (inductive)**
Rated line-to-line Voltage (RMS)	**400 [V]**
Filter	**L=10 [mH] R=100[mΩ]**
DC Link (C_{DC})	**5 [mF] / 700 V**
VOC with SV-PWM / VOC with MLV-PWM/ P-DPC based on 3+3 voltage vectors' sequence	
Switching Frequency (maximum)	**f_{swMAX}=2000[Hz]**
Control & Sample	**T_{sw}=1/ f_{swMAX}**

The control algorithms run under the SIMULINK/MATLAB environment in a dSPACE ds1103 real-time platform and the measurement system is based on a YOKOGAWA PZ4000 with a sample time of 2.5MS/s. The tuning of VOC-based controllers is based on the OS method (without prefilter), getting a first order dynamic behavior.

First, Fig.6.9 shows simulated per-phase switching signals and normalized per-phase current. Next, Fig.6.10 shows experimental per-phase converter's voltage related to negative point of DC-link and the line current. In the case of MLV-PWM and P-DPC there are no switching actions along the maximum of the line-current, therefore the overall switching losses are minimized. However, the efficiency improvement is related to current-spectrum deterioration, see Fig.6.11. The VOC-type SV-PWM strategy shows the best power quality (THD_i=4.10%), followed by the P-DPC (THD_i=4.84%) and the VOC-based MLV-PWM (THD_i=4.86%). As can be derived, both the P-DPC and MLV-PWM approaches minimize the switching losses with the same vector selection strategy, which leads naturally to a similar THD degradation. This THD penalization is an expected result considering that some degrees of freedom are not used in current control tasks. Nevertheless all strategies meet the IEEE Std 519-1992 recommendation.

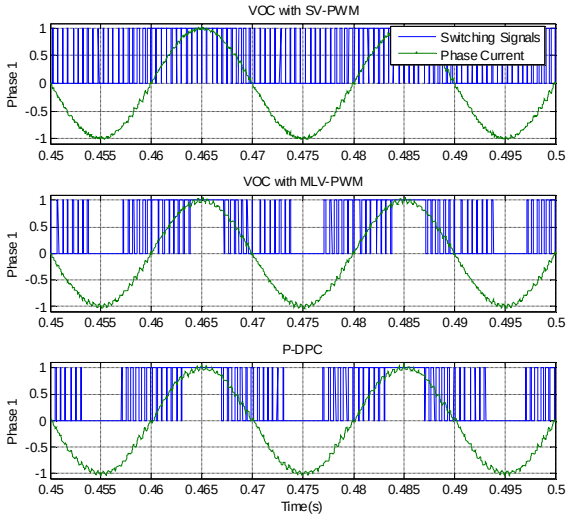
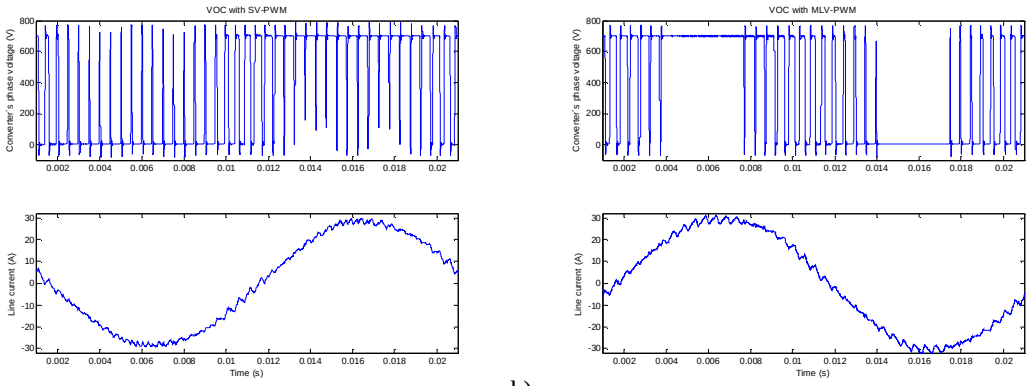
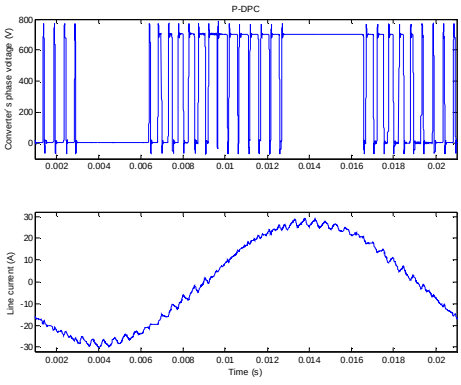


Fig.6.9: Simulated results of per-phase switching signals and normalized line current



a) b)



c)

Fig.6.10: Experimental results of per-phase converter's voltage related to negative point of DC-link and line current: a) VOC with SV-PWM, b) VOC with MLV-PWM, c) P-DPC

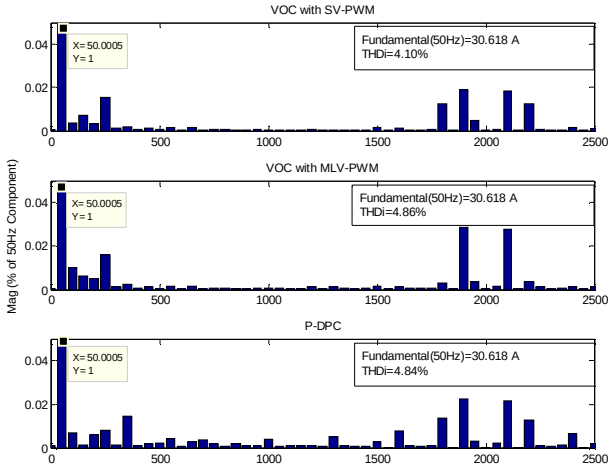
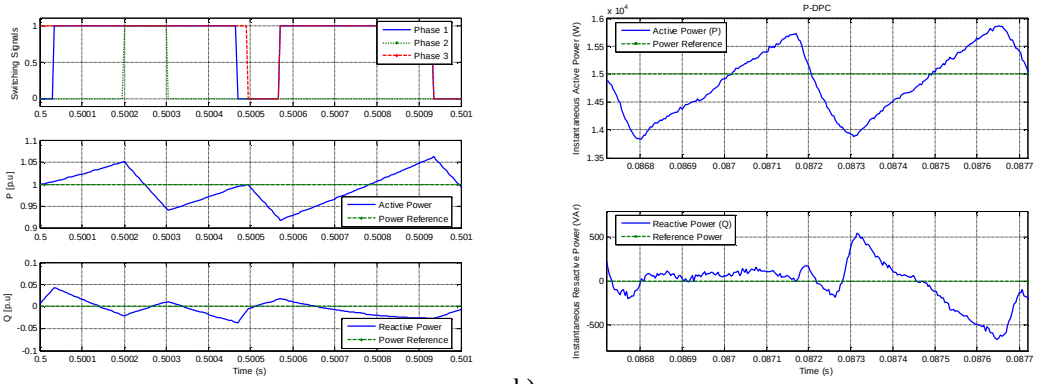


Fig.6.11: Experimental current frequency spectrum

Detailed behavior of simulated variables under P-DPC is shown in Fig.6.12a. In a similar way, Fig.6.12b reflects the experimental results of active and reactive power trajectories of two symmetrical 3+3 switching sequences. Two control periods are represented. As can be observed, quasi-linear active and reactive power trajectories evolve around the reference values, with a ripple of around 5%.



a) b)

Fig.6.12: Active and reactive power trajectories along two control periods: a) Simulated Results (Normalized values), b) Experimental results

The best P-DPC result is obtained, as expected, in transient behavior, see Fig.6.13. Two steps of active and reactive power references from zero to 15kW and 9kVAr have been applied. Though the P-DPC offers a slight improvement on reactive power transient, it is clearly faster in the active power tracking task, as it takes less than 5ms against the 60ms required by either of the two VOC strategies.

Fig.6.14 shows the experimental transient behaviors of active power and line current when an active-power reference step is applied at 0.08s. As can be observed the P-DPC transient takes only 5ms whereas

the VOC-based strategies need around 60ms to achieve the same transient. Logically, better transient responses in VOC can be obtained if current controllers design is optimized using a prefilter and feed-forwards loops (Chapter 3). This field has been developed in the experimental tests related to 3L-NPC VSI.

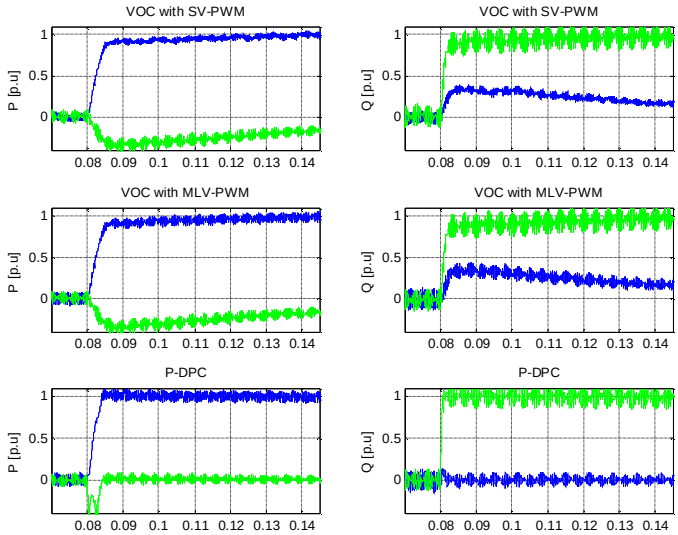


Fig.6.13: Instantaneous power behavior during active and reactive power reference steps (Normalized values)

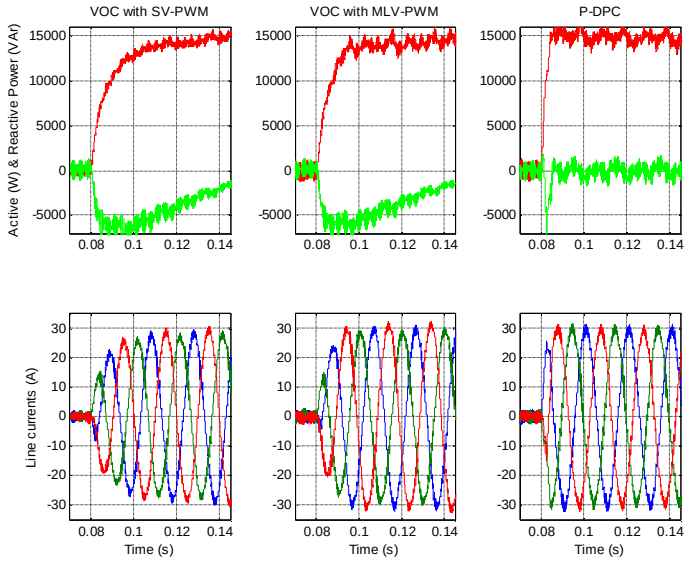


Fig.6.14: Experimental instantaneous power and current behaviors during active power reference steps

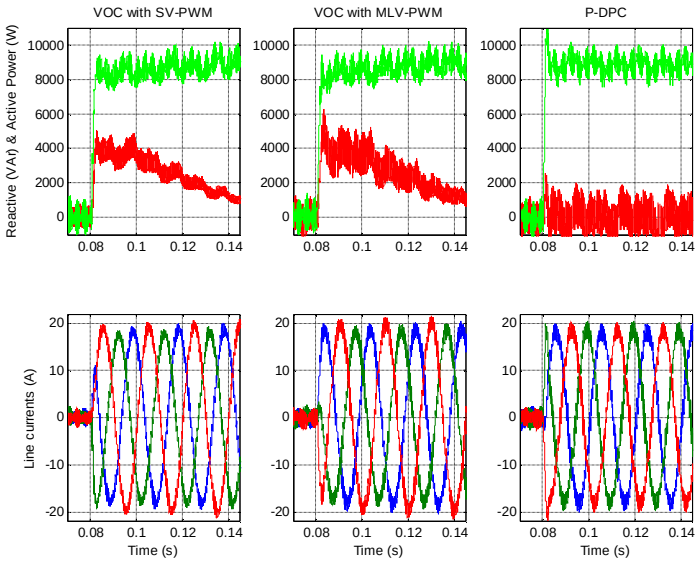


Fig.6.15: Experimental instantaneous power and current behaviors during reactive power reference steps

6.2.3. Comparative Study of the P-DPC and the VOC Strategy on a 3L-NPC VSI Operating as an Inverter

A comparison between the hybrid P-DPC and VOC strategies has also been carried out in a 3L-NPC VSI under 400V-15kVA operation conditions. The experimental platform consists of a three-level NPC inverter developed by SEDECAL and located at Faculty of Engineering of the University of Mondragon. Furthermore, a line inductor of 10mH, DC-link capacitors of 1.16mF each and a DC-supply are employed, see Fig.6.16. The main specifications of power and control systems are listed in Table 6.3.

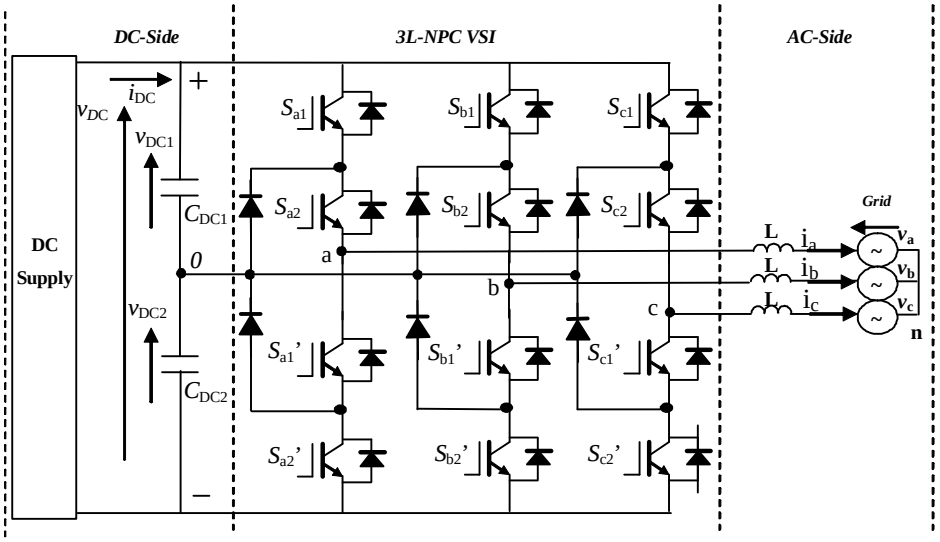


Fig.6.16: Electrical diagram. Laboratory platform of three-phase 3L-NPC VSI with a L-type filter under rectifier operation mode

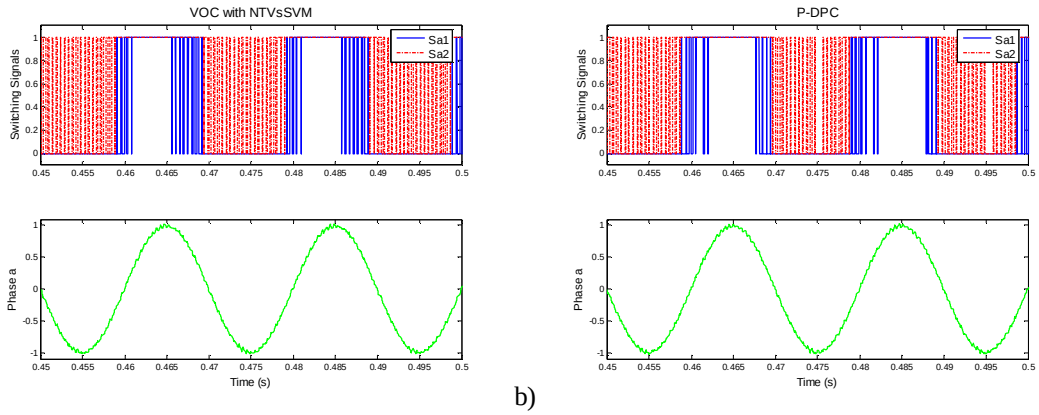
TABLE 6.3
SPECIFICATIONS OF POWER AND CONTROL SYSTEMS

	Value [unit]
Rated Power S_K	**15 [kVA] cosθ=0.8 (inductive)**
Rated line-to-line Voltage (RMS)	**400 [V]**
Filter	**L=10 [mH] R=100[mΩ]**
DC Link (C_{DC1}, C_{DC2})	**1.16[mF] / 700V**
VOC with NTV-SVM / Hybrid P-DPC	
Switching Frequency (maximum)	**f_{swMAX}=2000[Hz]**
Control & Sample	**T_{sw}=1/ f_{swMAX}**

As the previous case, the control algorithms run under the SIMULINK/MATLAB environment in a dSPACE ds1103 real time platform and the measurement system is based on a YOKOGAWA PZ4000 (sample time of 2.5MS/s) and Tektronix TPS 2024 200MHz. In order to generate the switching patterns the FPGA platform SPARTAN 3 is used. The tuning of the VOC-based controllers has been based on the OS method using a prefilter.

Fig.6.17 compares the simulated per-phase switching signals and normalized line-current of the VOC with NTV-SVM and the P-DPC strategy. In a similar way, Fig.6.18 shows experimental per-phase converter's voltage related to the neutral point of the DC-link and the line current. As can be observed there are no switching actions along the maximum of the line current, therefore the overall switching losses are minimized. The steady state is evaluated by THD measurements, see Fig.6.19. Both strategies present similar harmonic spectrum levels, near 2.4%, meeting the IEEE Std 519-1992 recommendation.

The P-DPC behavior along two control periods is shown in Fig.6.20. As can be observed, quasi-linear trajectories evolve around the reference values both in the simulation and experimental cases, with a ripple below 3%. Fig.6.21a outlines the evolution of the DC-link voltages and the neutral-error under P-DPC operation. The main harmonic is located at 150Hz, the typical characteristic of three-level converters with some kinds of SVMs. Fig.6.21b shows the experimental DC-capacitors' voltages ripples and line currents behavior under several active reference steps from 5kW to 10kW. It should be noted that the low frequency harmonic of around 5Hz under the DC-link voltages is related to the DC supply which has been used in the experimentation.



a) b)

Fig.6.17: Simulated results of per-phase switching signals and normalized line current: a) VOC with NTV-SVM, b) P-DPC

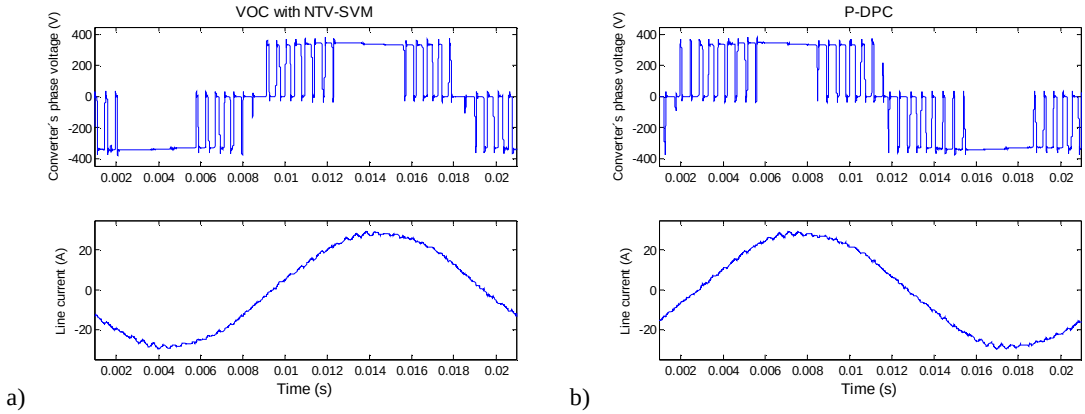


Fig.6.18: Experimental results of converter's per-phase voltage related to neutral point of the DC-link and line current: a) VOC with NTV-SVM, b) P-DPC

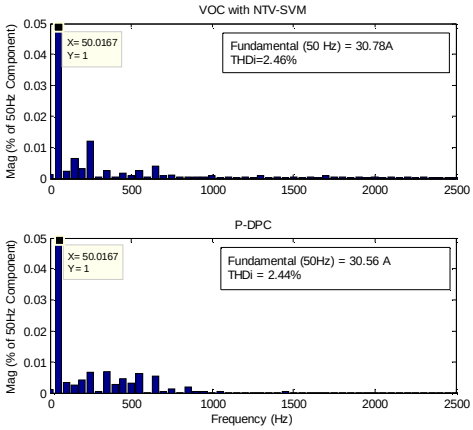


Fig.6.19: Experimental current frequency spectrum

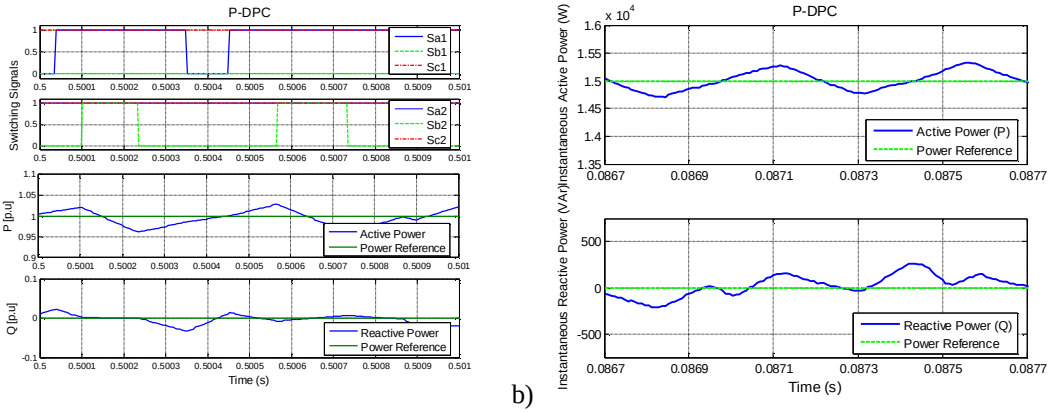
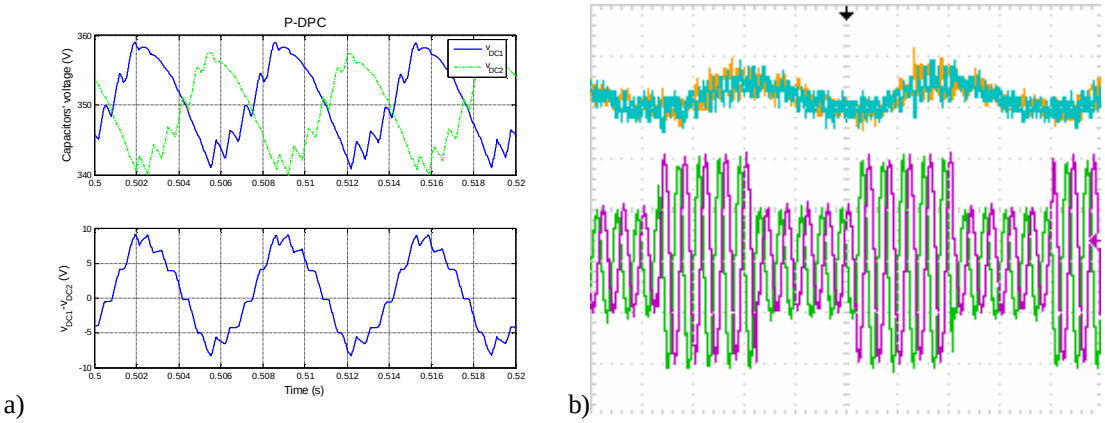


Fig.6.20: Active and reactive power trajectories along two control periods: a) Simulated Results (Normalized values), b) Experimental results

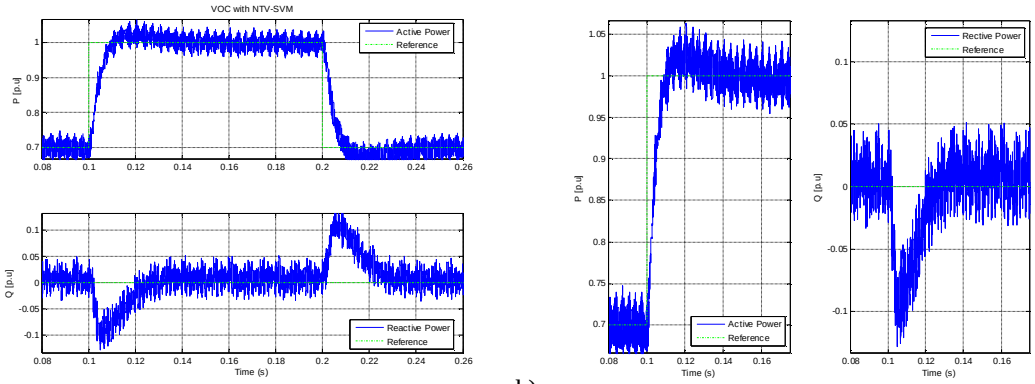


a) b)

Fig.6.21: a) Simulated DC-link voltages and error in the neutral point under the P-DPC operation, b) Experimental results of DC-link capacitors' voltage ripples and line currents under several active power reference steps

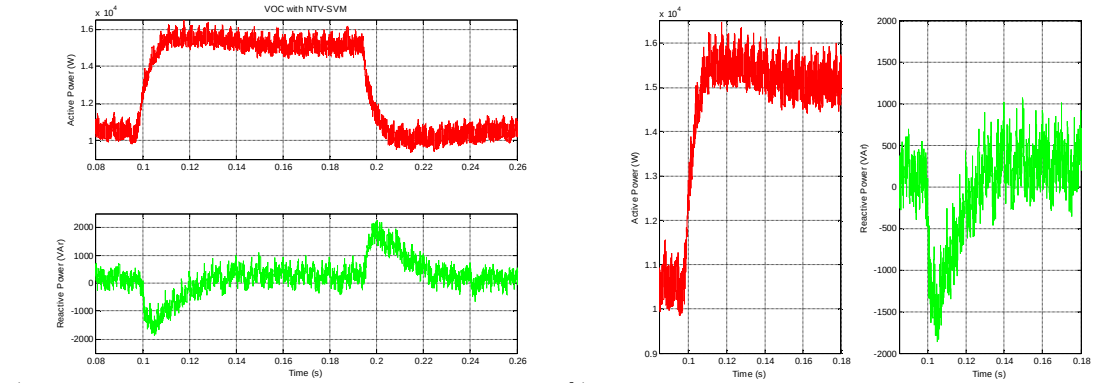
Oscilloscope: From the top DC-link capacitors' voltage ripples 20V/div, line currents 10A/div (time division of 50ms)

Finally, simulation and experimental results of the active and reactive power transient behavior under several reference steps from 10.5kW to 15kW (30%S_K) are shown in the following figures. The PI controllers of the VOC strategy (based on Park's *dq* Transformation) are tuned using optimal approaches, leading to a fast transient response of around 20ms. However, it is possible to observe an overshoot and the *dq* cross-coupling effect. On the other hand, the P-DPC strategy shows an improved transient behavior, obtaining a fast dynamic response below 4ms without any overshoot or cross-coupling effects.



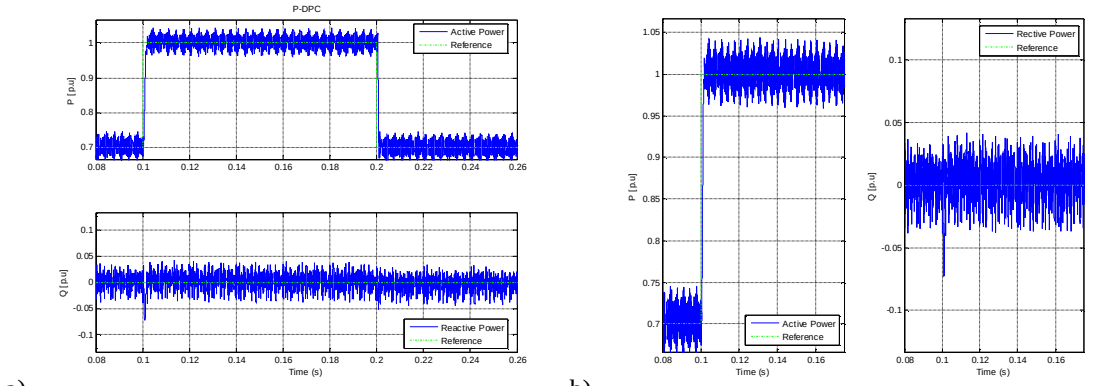
a) b)

Fig.6.22: VOC with NTV-SVM. Instantaneous power behavior during active power reference steps



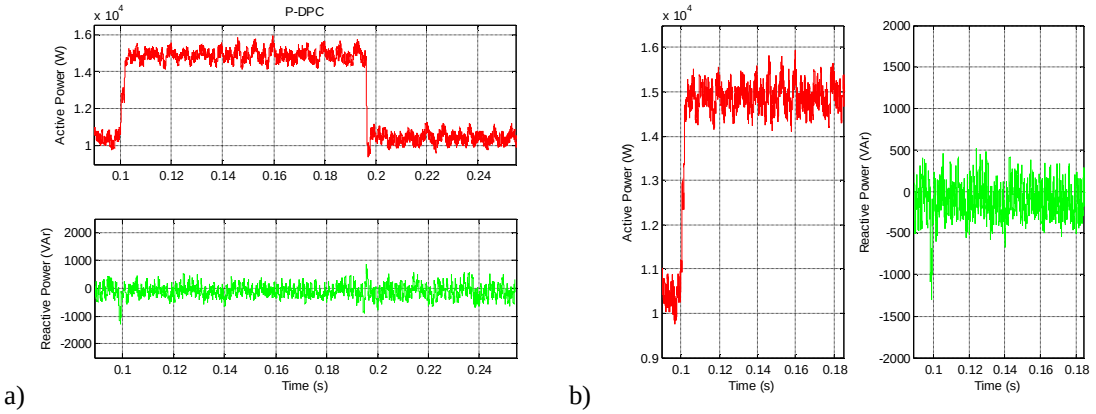
a) b)

Fig.6.23: VOC with NTV-SVM. Experimental instantaneous power behavior during active power reference steps



a) b)

Fig.6.24: P-DPC. Instantaneous power behavior during active power reference steps



a) b)

6.25: P-DPC. Experimental instantaneous power behavior during active power reference steps

6.3. Conclusions

In order to verify the behavior of the P-DPC algorithm, several simulations and experimental tests in different laboratory set-ups have been carried out. Concretely, this chapter evaluates both the symmetrical 3+3 vector's sequence and the hybrid version of P-DPC along with VOC strategies in a grid-connected 2L and 3L-NPC VSIs.

The P-DPC shows very good results both in steady-state and transients. The comparative study between standard VOC strategies with SV-PWM and MLV-PWM in the 2L-VSI establish that the P-DPC (based on symmetrical 3+3 vectors' sequence version) is several times faster in power transients. It offers the same power loss reduction in the steady-state as the MLV-PWM and therefore, the resulting THD is also penalized. In a similar way, the comparison between the VOC with NTV-SVM and the P-DPC (hybrid version) in the 3L-NPC VSI shows a similar harmonic spectrum levels in steady-state operation but improving the transient behavior.

These results are coherent with the fact that P-DPC strategies exploit the same set of voltage-vectors in steady-state operation and that the *d-q* cross-coupling affects the VOC-based systems in transients. Nevertheless, all control strategies analyzed in this Chapter meet the IEEE Std 519-1992 recommendation.

Chapter 7

7. Conclusions and Future Prospects

7.1. Summary

The frame of this thesis is the trend toward transformerless MV connection of power converters. This is the case of a large number of new active systems, such as wind turbines, hydraulic generators, biomass and geothermal generators, photovoltaic systems, FACTS devices and others. New developments in semiconductors allow an increase of their maximum voltage, current and switching frequency, in such a way that it is possible to design efficient and reliable VSIs for MV applications. Among these designs, the three-phase two-level VSI (2L-VSI) and three-level NPC VSI (3L-NPC VSI) configurations are mainly employed and therefore, this dissertation deals with the improvement of control of these devices. First the basic operation principles and several mathematical models of the VSI have been presented including some design considerations and establishing the main specifications and features of a grid-connected 2L-VSI and 3L-NPC VSI under 2.3kV-2MVA operation conditions.

Generally, these devices must provide a target active and/or reactive power level to the line, so appropriate Power Control systems are required. A classification of commonly employed control methods has been carried out, classifying them within two control groups; the indirect and direct power control techniques. Among the available indirect control strategies, the VOC is mainly utilized, so it has been retained in order to be considered in this dissertation. On the other hand, the direct control type DPC strategy shows attractive features related to fast transient behavior, employing active and reactive power tracking requirements. Hence, both control methods have been evaluated, developing a new control approach called Predictive Direct Power Control (P-DPC). This new control algorithm combines the DPC characteristics with a predictive selection of a voltage-vectors' sequence, obtaining both high transient dynamic and constant switching frequency. Different P-DPC versions have been proposed, involving the P-DPC based on an optimal application of two, three, symmetrical 2+2 and symmetrical 3+3 voltage vectors' sequences. In order to evaluate these control strategies several simulations of a grid-connected 2L-VSI and 3L-NPC VSI under a 2.3kV-2MVA operation performance have been carried out.

These first study and simulations have lead to the selection of the best behaved control strategies for MV grid-connection. This way, a performance comparison between the VOC techniques (with MLV-PWM and NTV-SVM strategies for the 2L-VSI and 3L-NPC VSIs respectively) and P-DPC algorithms (based on a symmetrical 3+3 voltage vectors' sequence) has been developed. This analysis has taken into account different situations including power reference steps, drifts of filter's inductance values and the influence of usual power system's disturbances.

Finally, several experimental tests of the 2L and 3L-NPC VSIs under P-DPC have validated the proposed approach.

7.2. General Conclusions

This research work proposes the Predictive Direct Power Control (P-DPC), a new control approach where the well-known direct power control is combined with a predictive selection of a voltage-vectors sequence, obtaining both high transient dynamic and constant switching frequency.

The first part of the dissertation, devoted to the analysis and design of MV converters, has shown that the 2L-VSI requires an extremely large inductor in order to fulfill the IEEE 519-1992 standard, leading to a high voltage drop in the filter and increasing the DC-link voltage requirements. Therefore, the 2L-VSI with L-type filter is not a useful MV converter topology if efficiency and low THD are required. Nevertheless, the 3L-NPC VSI requires smaller inductor's values (below 50% related to 2L-VSI-based design when similar power quality conditions are assumed), becoming a very interesting option for MV grid-connected applications.

One of the results of the analysis of the state-of-the-art of different modulation techniques is that the SV-PWM (with four voltage vectors per control period) shows the best power quality and the minimum DC-voltage ripple. The MLV-PWM, with three voltage vectors per control period, reduces the power losses significantly, which is particularly interesting for MV and high power applications. However, the improvement in power losses is related to current-spectrum and DC-link voltage deterioration. The 3L-NPC VSI with NTV-SVM also uses three voltage vectors per control period, but the power quality is better thanks to the multiplicity of voltage levels and the overall efficiency is optimized. Yet, its basic configuration suffers for the typical 150Hz perturbation in the capacitors' DC-voltages.

Comparing the state-of-the-art of VOC and DPC strategies, the best power quality and the smallest reference tracking error are assured by the VOC approaches. On the other hand, the DPC approach offers the fastest transients without overshoot and avoiding any cross-coupling.

Concerning the proposed P-DPC, the symmetrical 3+3 vectors' sequence leads to the best results for both the 2L and 3L-NPC VSI configurations. Nevertheless, only the 3L-NPC VSI meets the IEEE Std 519-1992 recommendation.

The performance comparison between the state-of-the-art of VOC techniques and the new P-DPC approach shows that the last one is an attractive option for grid-connected converters. Thanks to its direct-control structure it shows the best transient behavior, but, contrary to classical DPC approaches, the predictive strategy assures constant switching-frequency, which leads to the same power quality levels as the VOC type approaches. However, this algorithm is more sensitive against any drift on the value of the filter's inductance. These drifts do not damage the system's stability but they affect the current tracking error, especially on the case of the 3L-NPC VSI. In a similar way, the analysis of the influence of line-voltage harmonics shows that the P-DPC is more sensitive than the VOC-based strategies. In addition, this new approach is very sensitive to the voltage sags. The VOC techniques are also affected by these perturbations and especially in the 3L-NPC VSI configuration when unbalanced operation conditions are produced.

The experimental tests show very good results under different operation conditions, both in steady-state and in transients. The comparison between VOC-based strategies and the proposed approaches establishes that the P-DPC is several times faster in active-power reference transients and at the same time it does not deteriorate the steady-state harmonic spectrum.

In the author's opinion the thesis formulated in Chapter 1 has been proved. The proposed P-DPC algorithm could become an interesting alternative to standard VOC techniques for MV grid-connected converters.

7.3. Future Prospects

Important P-DPC improvements are possible. This is the case of the hybrid P-DPC algorithm which has been introduced in Chapter 4 and developed in Chapter 6. This P-DPC version uses a large set of concatenated-voltage vectors in steady state operation, improving the efficiency and current ripple, but at the same time it exploits the advantages of a simple set of two concatenated-voltage vectors in transients. Following this trend, new P-DPC versions combining different control strategies could be developed.

As shown in Chapter 5, the P-DPC is based on the knowledge of the system's model and therefore, it is sensitive to parameter drifts. A typical deviation in the filter's-inductance produces only small errors, so it will not damage the stability of the system. Anyway, the resulting non-expected error could be utilized in an on-line parameter's-estimation system, leading to an adaptive version of the P-DPC. In a similar way, this control approach shows a substantial sensitivity to line voltage harmonics and sags, so the addition of a PLL will probably solve most of the problems arising from these situations.

Finally, the extension of the P-DPC theory to other VSI-based systems using LC or LCL grid filters could be explored. In these cases, original predictive models of instantaneous power could be developed, establishing the new geometrical behaviors of active and reactive-power trajectories. This way, it is possible to reduce the switching frequency and increase the converter's power, becoming an attractive solution from the point of view of MV grid-connected applications.

A. Appendices

A.1 Coordinate Transformations

This research work employs the following Park's transformations to a rotating *dq0* reference frame and Clark's transformations to a static *αβ0* reference frame.

Clark's direct *abc/αβ0* and inverse *αβ0/abc* transformations:

$$\begin{bmatrix} X_a \\ X_b \\ X_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{A.1}$$

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} X_a \\ X_b \\ X_0 \end{bmatrix} \tag{A.2}$$

Park's direct *dq0/abc* and inverse *abc/dq0*transformations:

$$\begin{bmatrix} X_d \\ X_q \\ X_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin(wt) & \sin\left(wt-\frac{2p}{3}\right) & \sin\left(wt+\frac{2p}{3}\right) \\ \cos(wt) & \cos\left(wt-\frac{2p}{3}\right) & \cos\left(wt+\frac{2p}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{A.3}$$

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} \sin(wt) & \cos(wt) & 1 \\ \sin\left(wt-\frac{2p}{3}\right) & \cos\left(wt-\frac{2p}{3}\right) & 1 \\ \sin\left(wt+\frac{2p}{3}\right) & \cos\left(wt+\frac{2p}{3}\right) & 1 \end{bmatrix} \cdot \begin{bmatrix} X_d \\ X_q \\ X_0 \end{bmatrix} \tag{A.4}$$

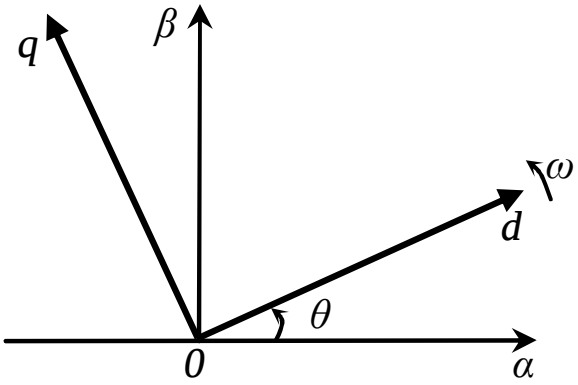


Fig.A.1: Relation between the Park's and Clack's reference frames

A.2 Harmonic Limits

IEEE 519-1992

It defines the limits for harmonic voltages and currents at the Point of Common Coupling (PCC)

TABLE A.1
VOLTAGE DISTORTION LIMITS

Voltage at PCC	Individual voltage distortion [%]	Total voltage distortion THD
< 69kV	3.0	5.0
69kV – 138kV	1.5	2.5
>138kV	1.0	1.5

TABLE A.2
MAXIMUM ODD HARMONIC CURRENT DISTORTION LIMITS IN PERCENT OF IL FOR GENERAL DISTRIBUTION SYSTEMS (120V-69kV)

I_{SC}/I_L	<11	11≤ h <17	17≤ h <23	23≤ h <35	35≤ h	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Here:

h is the harmonic order

$\mathbf{I_{SC}}$ is the maximum short circuit current at the PCC

$\mathbf{I_L}$ represents the fundamental current of the average (over 12 months) maximum monthly demand load current at PCC

TDD is the total demand distortion, harmonic current distortion as % of the maximum demand load current (15 or 30 minute demand)

IEC 61000-3-2

It refers to small customer equipment (public, low-voltage and household)

TABLE A.3
HARMONIC LIMITS FOR LV -CLASS D EQUIPMENT

Harmonic order (h)	**Maximum permissible harmonic current per watt (mA/W)**	**Maximum permissible harmonic current**
3	2.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13< h < 39 (only odd harmonics)	3.85/h	Refer to class A

IEC 61000-3-4

It refers to larger customer equipment (single and three-phase harmonic limits)

TABLE A.4
LIMITS FOR THREE-PHASE EQUIPMENT CONSIDERING THE SHORT CIRCUIT RATIO RSCC

Minimal R_{SCC}	**Upper limits for harmonic distortion factors**		**Limits for individual harmonic in % of I1**			
	THD	PWHD	I_5	I_7	I_{11}	I_{13}
66	17	22	12	10	9	6
120	18	29	15	12	12	8
175	25	33	20	14	12	8
250	35	39	30	18	13	8
350	48	46	40	25	15	10
400	58	51	50	35	20	15
>600	70	57	60	40	25	18

Here:

$$PWHD = \sqrt{\sum_{n=14}^{40}\left(\frac{I_n}{I_1}\right)^2}$$

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